Design of Ultra Low Drop-out Regulator for Audio Devices

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Abstract

Low Drop Out (LDO) regulators are widely used in battery-powered portable electronic devices because of their low dropout, low quiescent current and large load current characteristics with minimum heat losses. The proposed ultra LDO regulator architecture uses a telescopic error amplifier and single stage charge pump with non-over lapping clock logic. The telescopic cascode error amplifier with NMOS pass element output stage increases the Power Supply Rejection Ration (PSRR) of the ultra LDO regulator and also reduces the area by using internal compensation. The non-over lapping clock logic minimizes the charge pump losses, thus enabling the ultra-low drop out. The ultra-low dropout regulator design has been analysed its performance against the specification requirement for audio device applications and implemented in 180 nm CMOS technology. The results show the proposed ultra-low drop out regulator is capable of delivering 1.5V regulated output with 200 mA load current over supply voltage range of 1.95 V to 1.55 V with a bandwidth of 20 kHz. The drop out voltage is only 50 mV at maximum load current (200 mA) for minimum supply voltage. The load regulation is 0.1 mV/mA and line regulation is 1 mV/100mV. The ultra LDO regulator has a PSRR of -56 dB at 20 kHz. The area of the ultra low drop out regulator is 0.1 mm^2.

Key Words: Voltage Reference, Low Drop Out Voltage Regulator, NMOS Pass Transistor, Ultra- Low Drop Out Regulator

1. INTRODUCTION

The LDO regulator is widely used to provide reliable, constant output voltage to drive the sub-circuits of sensitive analog or audio blocks in the portable devices which needs stringent noise and PSRR requirements [1, 2]. The major challenge in LDO regulator design is to maintain stability across a wide range of load currents with low quiescent current. The block diagram of a conventional low drop out voltage regulator is shown in Fig. 1. It requires a large on board capacitor for stability compensation at the output and needs an external pin for a board mounted output capacitor which increases the area and reduces the bandwidth of the system [3]. This problem can be solved by using an NMOS device as the pass element in the LDO regulator which compensate the stability internally and eliminates the need of a bigger on board capacitor [4, 5].

The switched floating capacitor technique allows continuous operation of an on-chip NMOS-based LDO regulator with a simpler switching scheme. In order to perform low-dropout operation using NMOS, two different approaches are used to overdrive the NMOS gate. One is dynamic biasing and the other one is clock booster. A dynamic biasing strategy and a clock booster technique ensure adequate drive to the NMOS power transistor in a power efficient fashion and without limiting the speed response of the regulator [6].

In the NMOS based LDO, low output impedance leads to an easier regulation and thus to a lower current consumption of the regulator. Additionally, the NMOS device requires a smaller silicon area to deliver the same amount of current [7]. The floating gate technique is used to perform a low dropout operation. But this approach is requires a specific technique which must be programmed, resulting in an increased complexity of the regulator. To overcome this issue a charge pump is used to boost the gate voltage for the ultra LDO regulator. The small area, low power and elimination of large output capacitor make this design for audio application in battery operated devices like smart phones and tablets.

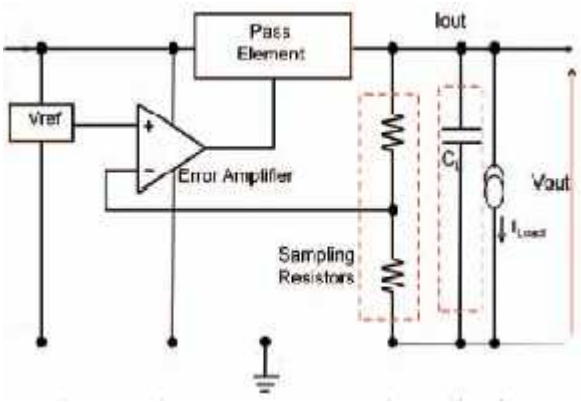

Fig. 1 Block Diagram of LDO regulator [1]

2. ULTRA LDO REGULATOR DESIGN

The block diagram of the proposed ultra low drop out regulator is shown in Fig. 2. The ultra-low drop out regulator consists of charge pump, error amplifier, and pass transistor. The pass transistor acts as variable resistor which maintains the output as 1.5 V. The pass transistor gate voltage is controlled by the error amplifier. The amplifier compares the feedback signal voltage with the 1.2 V reference and increases the voltage level to drive the gate voltage of the pass element to maintain the regulated output. The error amplifier requires 3.3 V to deliver the higher output voltage to drive the pass transistor. The charge pump acts as a

voltage doubler and provides required current and voltage for the amplifier. The proposed ultra LDO regulator design specification for audio applications is shown in Table 1.

Table 1. Ultra LDO regulator specification

Specification	Value
Power supply range	1.55 V to 1.95 V
Nominal supply	1.8 V
Regulated output	1.5 V
Dropout voltage	50 mV
Maximum load current	200 mA
PSRR	-50 dB at 20 kHz
Operating Frequency	20 Hz to 20 kHz
Area	0.1 mm^2

2.1 Pass Element Design

In this ultra LDO regulator, the NMOS pass element act as switch which delivers the required current and maintains the regulated output voltage. The maximum load current of the design is chosen to 200 mA.The regulated output voltage is fixed to 1.5 V. In this ultra LDO design, the NMOS pass transistor act in linear region because the drain to source voltage of pass element is less than the difference between gate to source voltage and threshold voltage of pass element ($V_{ds} < V_{gs} - V_t$). The W/L ratio of the NMOS pass transistor is calculated using the Eq. 1.

$$I_d = \mu n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \left(V_{ds}^2/2\right)\right] \qquad (1)$$

Where I_d is the load current, V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage, $\mu_n C_{ox}$ is the process parameter and V_{th} is the threshold voltage.

2.2 Error Amplifier Design

The error amplifier produces an error signal when there are difference between the sensed feedbacks output voltage and reference voltage. In this design, a telescopic cascade amplifier is used for its lower power consumption, easier compensation and high gain. The maximum load capacitance is calculated as 4pf (C_{gd}) for 25 kHz bandwidth audio application. The proposed telescopic cascade amplifier schematic diagram is shown in Fig. 3. The PSRR of an LDO regulator can be written as

$$PSRR = 20\log\frac{A_v}{A_{vo}}$$

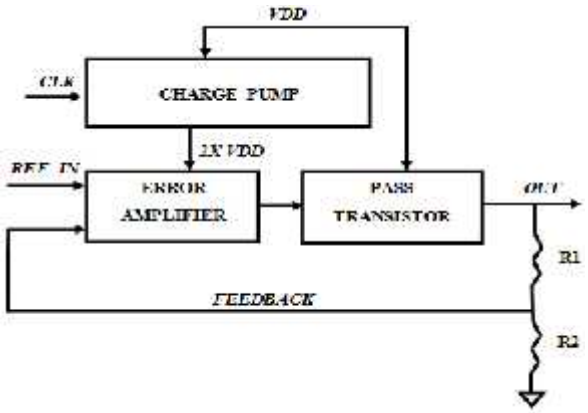

Fig. 2 Block diagram of proposed ultra-low drop out regulator

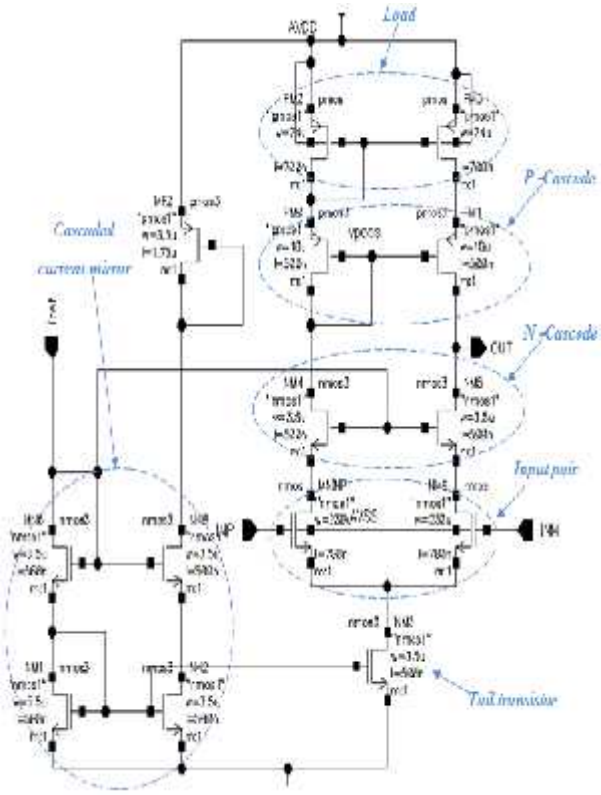

Fig. 3 Schematic of error amplifier

Where A_V is the open-loop gain of the regulator feedback loop, and A_{VO} is the gain from V_{IN} to V_{OUT}. Tail current is calculated using Eq.3

$$SlewRate = \frac{Tailcurrent}{C_L}$$

Where slew rate is 2.5 V/100µs and load capacitor is 3pf. The calculated tail current is 30 µA.The trans-conductance and size of input pair is designed using Eq.4

$$UGBW = \frac{g_m}{C_L}$$

$$g_m = \sqrt{2I_{tail} * k * \frac{W}{L}}$$

Where UGBW is the unity gain bandwidth, g_m is the trans-conductance, C_L is the load capacitor, I_{tail} is the tail current and K is the process constant.

2.3 Charge Pump Design

In this ultra LDO regulator, the charge pump acts as a voltage doubler. The schematic diagram of the charge pump is shown in Fig. 4. The 50 MHz clock is used as input to the non-overlapping clock logic. The minimum supply voltage to bias the amplifier is 2.8 V. The ripple voltage of 100 mV is chosen. The maximum peak of charge pump output would be 3.2 V and minimum charge pump output would be 3.1 V using the Eq.6.

$$V_{ripple} = V_{\max} - V_{\min}$$

$$CF = \frac{I_{load} * T}{V_{\max} - V_o}$$

Where Iload load current, T is the time period of the clock, V_o is the nominal output of the charge pump. The Output capacitor is decided as 23 pf using the Eq. 8.

$$CL = \frac{I_{load} * T/2}{V_o - V_{\min}}$$

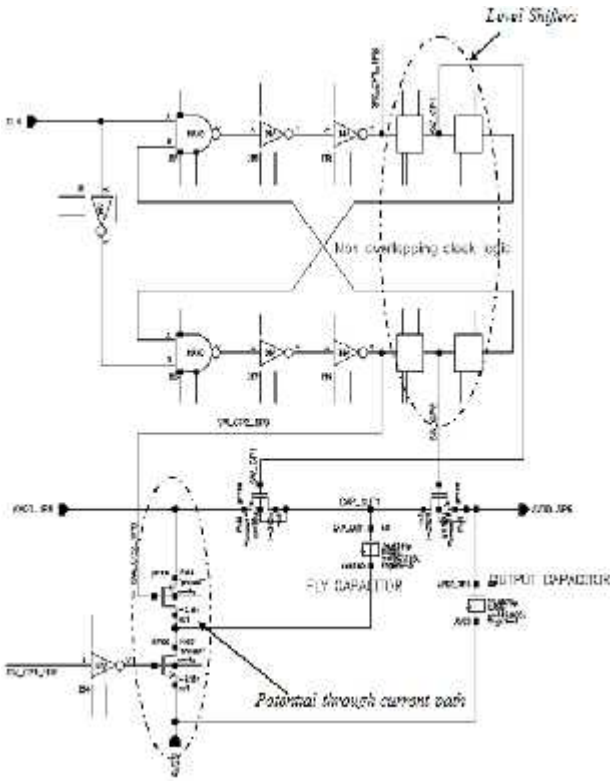

Fig. 4 Schematic diagram of charge pump

2.4 Top Level Design of Ultra LDO Regulator

The top level ultra LDO are designed by integrating sub-circuits like error amplifier, charge pump, a pass transistor and feedback resistor divider. The feedback resistor dividers R_0 and R_1) ratio is chosen for output voltage to maintain 1.5V and to reduce the quiescent current of regulator. The R_0 and R_1 values are 70KΩ and 280KΩ respectively. The resistor R_4 (70 KΩ) is added to series with the compensation capacitor to reduce the voltage drop caused at the pass element gate voltage. The top level schematic diagram of ultra LDO regulator is shown in Fig. 5.

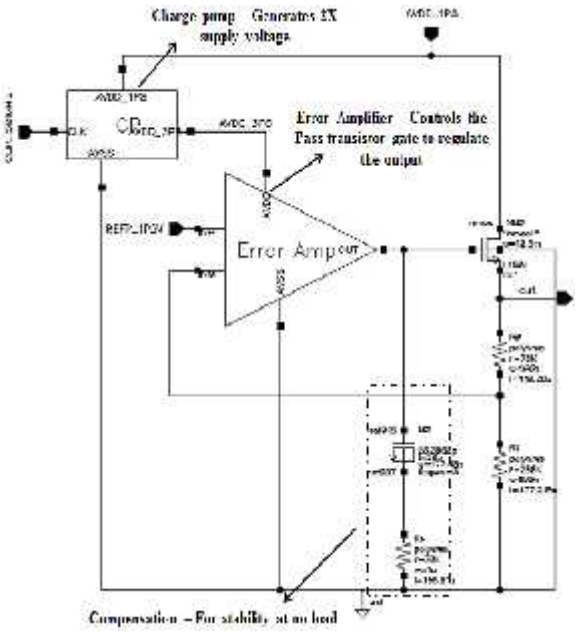

Fig. 5 Top Level Schematic of ultra LDO regulator

3. RESULTS AND DISCUSSIONS

The LDO regulator is simulated and results are analyzed for load capacitance of 100pf by varying resistance from 7 Ω to 700 kΩ. The input supply voltage is varied from 1.55 V to 1.95 V. The stability analysis is performed from maximum resistive load to no resistive load condition.

3. 1 Performance Characteristics of LDO regulator

The simulated transient response of the LDO regulator by varying load temperature and supply voltage is shown in Fig.6. This result shows that the LDO regulator meets the specification of regulated output voltage (1.5 V) for maximum and minimum supply voltage 1.95 V and 1.55 V respectively.

The ultra LDO regulator simulation result shows an output voltage of 1.48 V and it is capable of delivering 211 mA of current for supply voltage of 1.55 V. The load regulation result shows the variation of the LDO regulator output with variation in output current and measured 0.1 mV/mA. The line regulation is measured 1 mV/100mV. The power supply rejection ratio of LDO regulator is -56 dB at 20 kHz.

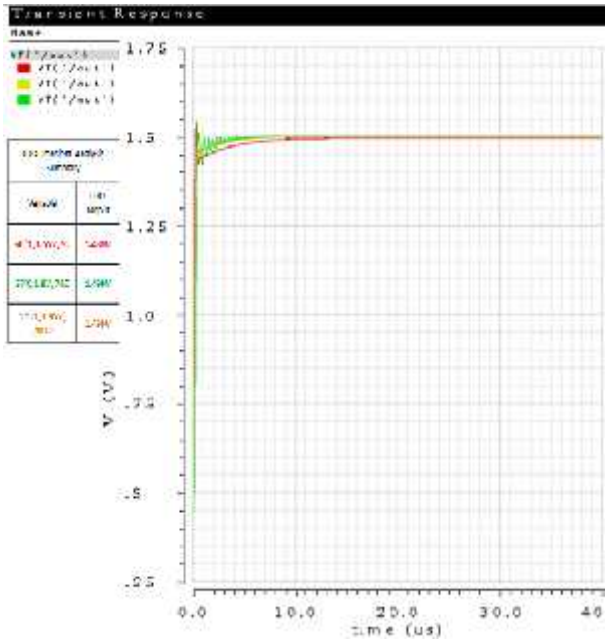

Fig. 6 Ultra LDO output with variation in temperature, load and supply

The layout of the LDO regulator is implemented in TSMC 180 nm CMOS technology using Cadence Virtuoso. The top level layout of the LDO regulator is shown in Fig. 7. The area of the LDO regulator is 0.1 mm^2 for 200 mA load current. The area of the LDO regulator is dominated by the pass transistor.

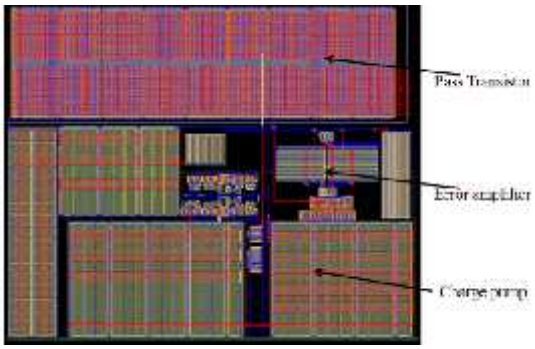

Fig. 7 Top level layout of LDO regulator

4. CONCLUSIONS

In this proposed ultra low drop-out regulator, by using an NMOS transistor as pass element, the internal compensation is achieved which eliminates the need of an on board capacitor and also an extra pin in the package of SOC. This saves the area and cost of the system. The telescopic cascode amplifier is used to reduce power consumption and improve the PSRR of the ultra LDO regulator. The single stage charge pump output is used as power supply for error amplifier. The error amplifier overdrives the NMOS pass transistor gate which regulates the output voltage. The non-overlapping clock logic is reduced losses in charge pump which in turn enabled the error amplifier to work in lowest supply of 1.55 V. The designed ultra low drop out regulator is capable of delivering 1.5 V regulated output with 200 mA load current over the supply voltage range from 1.95 V to 1.55 V. The drop out voltage is only 50 mV at maximum load current (200 mA) for minimum the supply voltage.

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