Validation of Low Power Format using Standard Cell Library

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Abstract

Increased system complexity has led to the substitution of the traditional bottom-up design flow by systematic hierarchical design flow. With decreasing channel lengths, few key problems such as timing closure, design sign-off, routing complexity, and power dissipation arise in the design flows. Specifically, minimizing power dissipation is critical in several high-end processors.

This research aims at optimizing the design flow for power using the unified power format (UPF). The low power reduction techniques enforced in this research are multivoltage, multi-threshold voltage (Vth), and power gating with state retention. A top-down digital design flow for a flash based mixed signal microcontroller has been implemented with and without UPF synthesis flow for 45nm technology. The UPF synthesis is implemented with two voltages, 1.2V and 0.9V (Multi-VDD). Area, power and timing metrics are analyzed for the flows developed.

Power savings of about 20 % are achieved in the design flow with 'multi-threshold' power technique compared to that of the design flow with no low power techniques employed. Similarly, 31 % power savings are achieved in the design flow with the UPF implemented when compared to that of the design flow with 'multi-threshold' power technique employed. Thus, a cumulative power savings of 51% has been achieved in a complete power efficient design flow (UPF) compared to that of the generic top-down standard flow with no power saving techniques employed.

Key Words: Low Power Format, Cell Library, Unified Power Format, signal microcontroller.

Nomenclature

MHz	mega Hertz
mSec	milli Second
mVolt	milli Volt
mW	milli Watts
nSec	nano Second
nW	nano Watts
nm	nano meter
pF	pico Farad
pSec	pico Second
uSec	micro Second
µW	micro Watts
V	volt

Abbreviations

CPF	Common Power Format
CPU	Central Processing Unit
DRC	Design Rule Check
DSP	Digital Signal Processor
EDA	Electronic Design Automation
IEEE	Institute for Electrical and Electronic Engineers
LVS	Layout Versus Schematic
MVRC	Multi Voltage Rule Checker
NMos	N Type Metal Oxide Semiconductor Device
PERL	Practical Extraction and Reporting Language
PMos	P Type Metal Oxide Semiconductor Device
RTL	Register Transistor Logic
SoC	System on Chip
UPF	Unified Power Format
Vth	Threshold Voltage

1. INTRODUCTION

The demand for low power drives the low power implementation techniques, UPF being the latest and most popular of the standards used for low power implementation, the need for a standard method for migrating an existing design to low power using UPF is very much in demand and the lack of any study on the impact of low power techniques on the design's power and area parameters are demanding such a study. In this study flash based mixed signal microcontroller design has been synthesized as a non-low power design and a low power design using UPF and compared the power, area and timing parameters of both designs. To verify and confirm the synthesis results, the design is also synthesized with third party tool power artist. To understand the effect of routing capacitance, physically implantation of flash based mixed signal microcontroller is also carried out using non-low power design and the results are compared with synthesized non-low power design. ASIC flow will be mimicked in this chapter using "**Flash based mixed signal microcontroller**" in 45nm IP library, the chapter contains complete design and simulations of the flash based mixed signal microcontroller. As the use of electronic devices pervades virtually every aspect of our lives, reducing power consumption must start at the semiconductor level. The power-saving techniques that are designed in at the chip level have a far-reaching impact. This is especially true with regard to the microcontrollers (MCUs) that serve as the intelligent engines behind a majority of

today's electronic devices. From a systems architecture perspective, the challenges of identifying which MCUs section are truly "low-power" sections.

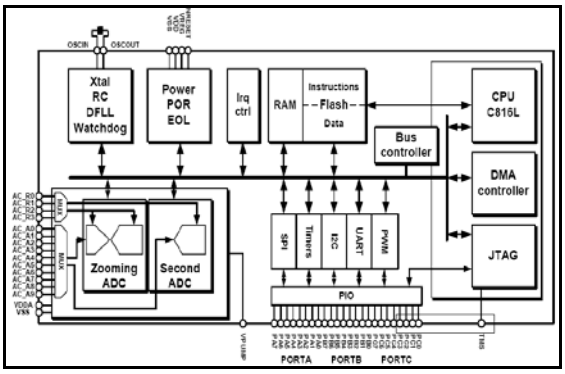

Fig. 1 Flash microcontroller (Open Cores, n.d.)

Power management has become the primary concern for designers, more and more designs are getting migrated to low power; UPF being the latest and widely accepted standard for low power implementations and power gating being the most efficient low power technique in use, a standard flow for migrating an existing design to low power using UPF and power management cells is needed to be developed. There have been studies on the accuracy of results between low power implementations using the standards like CPF and UPF and traditional low power implementation methodology. The comparison of results between a non-low power and low power implementation of same design remains unstated in the literatures, it is important from a designer's perspective to understand the impact of power management cells on the power and area compared to the non-low power implementation of the same design to choose the right low power technique for a particular application and this is the motivation behind choosing this work.

There have been several power management techniques evolving for past several years, most of which are matured technologies and a few are getting matured.

Clock Gating –A technique used to disable selected clock network to reduce dynamic power.

Gate Level Optimization –A technique used to reduce dynamic power by optimizing gates in a way that will connect high activity net to low power input and low activity net to high power input, thus reducing the power consumption.

Frequency Scaling – Reducing frequency reduces power consumption, frequency scaling is a technique to vary the frequency of operation dynamically when speed is not the prime constrain.

Multi VDD Design – Multi VDD design also known as voltage scaling technique is used in designs where different blocks can be operated at different voltages thus making most of the blocks work at lower voltage reducing the total power consumption.

Multi Threshold Logic – Leakage is inversely proportional to threshold voltage. Low Vth design will have high leakage and High Vth will have lowest leakage. Using Low Vth in performance critical path and High Vth in non-timing driven paths could reduce the leakage power considerably.

Power Gating – A technique where selected blocks in a design are shut down when they are not in use to reduce dynamic as well as leakage power. This is the most efficient power management technique in terms of power reduction but has a small impact on the timing as the entries in to shut down mode and wake up mode need to go through certain power-down and power-up sequences, which would consume a little time.

As mentioned earlier power gating is the most efficient power reduction technique because supply to the selected blocks is turned off when not in use. A lot of work has been done and are being done to improve the power gating methodology and implementation. One challenge that could come up with power gating is that the switching power supply may ramp-off very slowly leaving the devices at threshold voltage for a significant amount of time. This would result in large crowbar currents in always-powered blocks. The solution for this is to use special isolation cells which are designed not to experience any crowbar current even if one of the inputs are at threshold voltage unless the enable signal is off. In many cases it is highly desirable to retain the register states of the powered down block to get back to the old state quickly when the block is turned back on. Specially designed retention latches could be used to full fill this functionality.

The demand for low power drives the low power implementation techniques, UPF being the latest and most popular of the standards used for low power implementation, the need for a standard method for migrating an existing design to low power using UPF is very much in demand and the lack of any study on the impact of low power techniques on the design's power and area parameters are demanding such a study. In this study flash based mixed signal microcontroller design has been synthesized as a non-low power design and a low power design using UPF and compared the power, area and timing parameters of both designs. To verify and confirm the synthesis results, the design is also synthesized with third party tool power artist. To understand the effect of routing capacitance, physically implantation of flash based mixed signal microcontroller is also carried out using non-low power design and the results are compared with synthesized non-low power design.

2. DESIGN

As shown in Fig. 2 the proposed design flow contains mainly four sections

Section 1: RTL synthesis of flash based mixed signal microcontroller using 45nm standard cell library in Dc_shell tool. The design is synthesized in Dc_shell using standard cell libraries and no power management cells have been used. Front-end views Verilog and liberty

files have been used in RTL synthesis and later the synthesized netlist will be verified in modelsim tool and results like area, power and timing have been analyzed in detail using PTPX tool. The synthesized netlist is gate level netlist and it doesn't contain any RC data

Section 2: RTL synthesis of flash based mixed signal microcontroller using 45nm power management library and UPF files in DC_shell tool. This section is main high light of the study where power management cells have been used along with UPF files. Since UPF file and power management cells has been used it can be expected great improvements in power compared to standard cell synthesized netlist discussed in section-1.

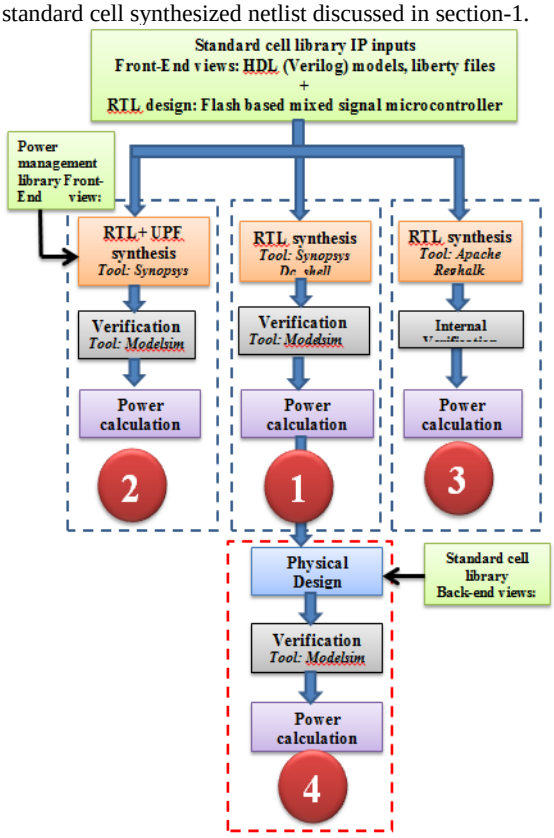

Fig. 2 Proposed design flow

Section 3: RTL synthesis of flash based mixed signal microcontroller using 45nm power management library in power artist tool. The power artist tool is much matured in synthesizing the RTL netlist tool with respect to power. The synthesis is purely based on power effort and great power improvements can be seen in this section. The area is least considered in this tool and hence the area value may get affected comparing the section-1 and section-2.

Section 4: Physical design implementation of RTL synthesized netlist of flash based mixed signal microcontroller using 45nm standard cell library. The synthesis netlist is borrowed from section-1 and further done physical implementation on the netlist, 45nm PDK is used in physical implementation. Since the physical implemented netlist contain the routing capacitance and also the gate level capacitance, the results have been very close to silicon results and it can be expected big value for power and area compared to all the 3 sections discussed above.

2.1 Importance Result Comparison

Section-1 and section-2: In both section-1 and section-2 the same RTL netlist is used for synthesis but the inputs for the synthesis have been different. In section-1 only standard cell library (without power management cell) have been used so, the synthesis netlist contains only standard cells and no power management cells. In section-2 the both power management cells and UPF files have been used hence the synthesized netlist contains power management cells. By comparing section-1 and section-2 it can be estimated how much power reduction is achieved using power management cells and UPF files and the power results will also help designer to take decision to go with only standard cell based design or power management based design. Since the power management cell area is bigger than the standard cells it can be expected increase in area number for power management based results. Thus these results will give broader picture to designer on how much percentage of power increase/decrease, area increase/decrease he can gain/loose with his design.

Section-2 and section-3: In both section-2 and section-3 the same RTL netlist is used for synthesis, even the same inputs (power management cells along with UPF files) have been used but the tool which have been used for synthesis are different. In section-2 Synopsys Dc_shell is used and in section-3 Apache redhalk power artist tool is used. The basic intention of using two different tools is: if any methodology/flow/algorithm problem with one tool will be easily caught by other tool by comparing the results (like power, area and timing). Here in this study if you see the Fig 2 All section-1, section-2 and section-4 have been using the tools from same EDA vendor (Synopsys) if by chance there is a bug in methodology/flow/algorithm it will propagate to all section-1, section-2 and section-4 because all are from same EDA vendor. So comparing section-2 and section-3 will give a broader picture to designer that how much margin he can see in the results and if it is well within the boundary both tool are fine to proceed or if both tools shows huge results then design may be wrong, or both results have been out of margin, any one tool is not functioning properly and that makes you further ping the EDA vendor.

Section-1 and section-4: In both section-1 and section-4 the same inputs have been used and those have been from standard cell library (which doesn't contain power management cells) the output from section-1 is gate level netlist (without RC information) the section-4 output result is gate level netlist with RC component and it also has routing capacitance. The section-4 takes more time to execute and it is the most time consuming step in ASIC design flow. The section-4 results have been closely match with silicon results as it accounted all parasitic and even the switching activities of all the nets in the design, because of the above mentioned reasons it can be expected big difference in results between section-1 and

section-4 but the results will actually give broader picture to designer on accounting the parasitic contents in early design phase that is after section-1.

2.2 Section-1

As shown in Figure 2. RTL synthesis of flash based mixed signal microcontroller using 45nm standard cell library in Dc_shell tool. The design is synthesized in Dc_shell using standard cell libraries and no power management cells have been used. Front-end views Verilog and liberty files have been used in RTL synthesis and later the synthesized netlist will be verified in modelsim tool and results like area, power and timing have been analyzed in detail using PTPX tool. The synthesized netlist is gate level netlist and it doesn't contain any RC data. The register-transfer level verilog code for a desired design or functionality is written and synthesized followed by a detailed placement and routing to obtain the physical layout for the design. Apart from the logic synthesis and physical design being important sections of the flow, it is also of equal importance to perform timing signoff and power signoff on the designs. Timing signoff check is done to ensure that the critical path in the design is well within the speed constraints specified at the initial stages of developing the functional description. Power signoff check is done so that the estimated power dissipation in the chip is on acceptable levels.

2.3 Section-2

RTL synthesis of flash based mixed signal microcontroller using 45nm power management library and UPF files in DC_shell tool. This section is main high light of the study where power management cells have been used along with UPF files. Since UPF file and power management cells have been used it can be expected a great improvements in power compared to standard cell synthesized netlist discussed in section-1. As shown in the above Fig 2 the front-end UPF files are major inputs for the design flow. Let us see these UPF creations for power management library and later for top level design, flash based mixed signal micro controller.

The following Fig 3 shows the block diagram of the Lib2upf tool. First the user needs to decide with the cellist and later the same cellist should be feed to the tool based on the cellist the appropriate UPF template files will be picked by the tool and later tool will looks for the specifications, since template files are technology independent all the data which are dependent on technology (Ex. Main supply voltage, back-up supply voltage etc.) will be picked from the design specifications.

2.4 Section-3

RTL synthesis of flash based mixed signal microcontroller using 45nm power management library in power artist tool. The power artist tool is much matured in synthesizing the RTL netlist tool with respect to power. The synthesis is purely based on power effort and great power improvements can be seen in this section.

The area is least considered in this tool and hence the area value may get affected comparing the section-1 and section-2. Power artist is a power sythesis tool from Apache Readhalk EDA vendor. Following are the capabilities of power artist tool

- Power-Performance-Area Trade-offs
- Voltage/Power Domain Planning
- Clock Gating: Block, Register, Memory
- Eliminating Redundant Activity
- Power Switch Sizing/Placement
- Level Shifters/Isolation cells
- Power Integrity Verification

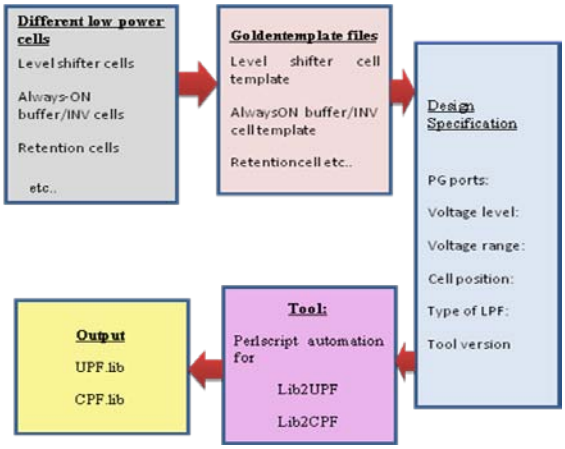

Fig. 3 UPF creation flow for Power management cell

2.5 Section-4

As shown in Figure 4 the physical design implementation of RTL synthesized netlist of flash based mixed signal microcontroller using 45nm standard cell library (the library doesn't include any power management cells). The synthesis netlist is borrowed from section-1 as mentioned in chapter-5 and further done physical implementation on the synthesized netlist, 45nm PDK is used in physical implementation. Since the physical implemented netlist contain the routing capacitance and also the gate level capacitance, the results have been very close to silicon results and it can be expected a big value for power and area compared to all the three sections.

Post synthesis, the consequent step to develop the design flow is to physically layout the optimized netlist of the design using the physical implementation tools. Since this research aims at developing a complete Synopsys flow, the Synopsys tool used for physical implementation is the IC compiler. Most commonly known Synopsys tools that enable us to place and route a given design have been Astro, Jupiter and IC Compiler. The IC Compiler is a single, convergent, chip-level design tool that enables designers to implement high-performance, complex and challenging designs. As a widely adopted solution, IC compiler provides best-in-class Quality of Results (QoR), tight sign-off correlation and powerful design for yield capabilities.

Results for top-down digital design flow				
Section	Flow steps	Area (sq. µm)	Power (mW)	timing (ns)
1	Synthesized	70275.85	0.746	0.01
4	Route_opt	75626.2	1.376	0.08

Table 1. Full system RTL design synthesis results

3 RESULTS AND DISCUSSIONS

3.1 Area Comparison

By looking at the Figure 5 and Figure 6 following discussion points can be made:

- Standard cell library synthesized netlist has less area number: synthesis did not consider any floor plan
- By comparing section-1 and section-2 there is almost 5% higher area is consumed by the UPF synthesis design this is because - the section-2 uses the power management cells along with UPF files and power management cell's area is higher compared the standard cells which were used in section-1.

Results for top-down digital design flow				
Section	Flow steps	AREA (sq.µm)	POWER (mW)	TIMING (ns)
1	Synthesized	70275.85	0.746	0.01
2	UPF synthesis	74018.88	0.3664	0.15
3	power artist synthesized	74823.68	0.33	0.11

Table 2. Full system RTL synthesis and PD results

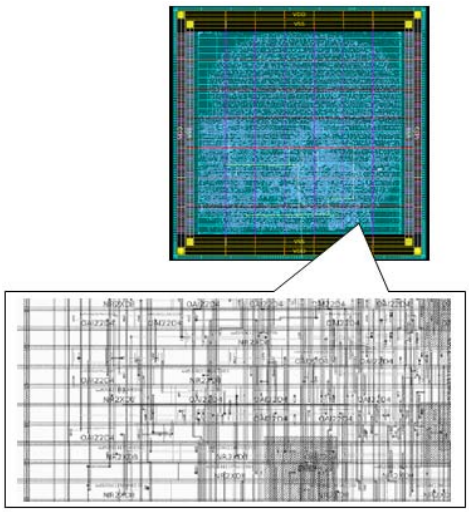

Fig. 4 Fully routed flash microcontroller

- By comparing section-1 and section-3 observe that the area consumption is more compared to section-2 this is because - in section-3 it has been used power artist tool to synthesize the netlist and this is power intent tool and is very poor in optimizing area
- By comparing section-1 and section-4 observed that the area consumption is worst this is because – the tool considers only the area of placed gates in the core leaving aside any white spaces whereas synthesis did not consider any floorplan, Usually the practice is to keep this margin as 10% for safer design flow.
- The results have been useful in comparing the cross-over sections i,e example comparison between section-2 and section-4, it can't be directly compare the results as because section-2 uses power management libraries and section-4 uses standard cell libraries for implementation and is post-synthesis netlist with RC components involved. But one can compare section-1 and section-2 because they have been with same RTL synthesis level and later the values can be extrapolated with section-4. Thus it can be expected more than 10% (may be 15% to 20%) area consumption of UPF implemented design.
- By comparing sction-2 and section-3, section-3 consumes more area it means, even though the inputs for RTL synthesis have been same (power management cells + UPF) the tools have been different. Section-2 it is Synopsys's Dc_shell and in section-3 it is Apache's Readhalk power artist tool. Since power artist is more focus is to optimize the power the area will take lower side and thus more area number and it is observed as almost 1% which is very small.

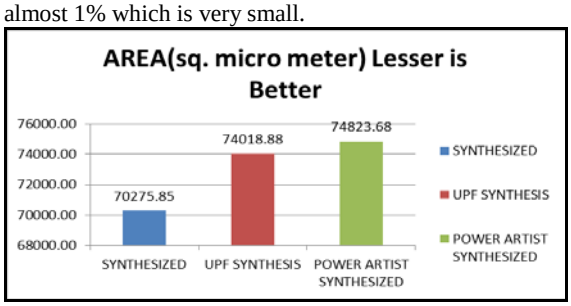

Fig. 5 RTL synthesis design area comparison

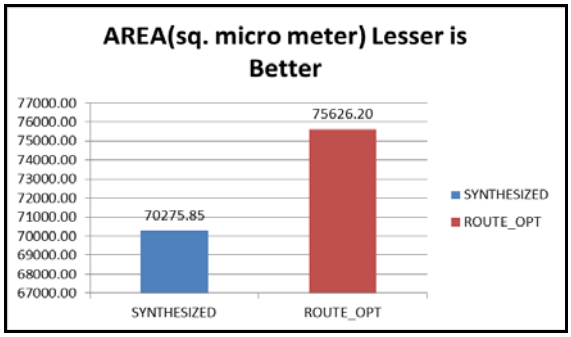

Fig. 6 RTL synthesis and PD area comparison

3.2 Power Comparison

By looking at Fig 6 and Fig 7 following discussion points can be made:

Section-3 consumes very less power this is because – in section-3 the RTL netlist is synthesized using power management cells + UPF files and the tool used is the

power artist which is intended to focus only on power optimization keeping area and timing in lower priority.

By comparing section-1 and section-2 observed that section-2 consumes less power as less as around 51% lesser than section-1 and this is because – in section-2 power management cells have been used + UPF files whereas in section-1 only standard cells have been used. Here the tool which is used for the synthesis in both sections have been same and is Dc_shell.
Section-1 and section-3 shows that section-3 consumes very less power as low as 55% and this is because - in section-3 power management cells + UPF files have been used whereas in section-1 only standard cells have been used. And the tool used is the power artist which is intended to focus only on power optimization keeping area and timing in lower priority.
By comparing section-1 and section-4 observed that RC capacitance is very dominating is design flow and it is as high as 84% comparing to RTL synthesized power number. Firstly, considering any switching activity and secondly due to the significant number of cells and routing head added in the physical design phase which will contribute to the power. Besides these reasons, when floor planning the design, the placement of the power pads and laying out the power buses will contribute the final power. Therefore, a significant increase in the routing power is observed when compared to the power reported out of DC.
By comparing sction-2 and section-3, section-3 consumes less power as less as 10%, it means even though the inputs for RTL synthesis have been same (power management cells + UPF) the tools have been different. Section-2 it is Synopsys's Dc_shell and in section-3 it is Apache's Readhalk power artist tool. Since power artist is more focus is to optimize the power and the area and timing will take lower.
If it is required to estimate the power consumption after physical implementation using power management cells + UPF files then need to extrapolate the numbers and the number can be roughly estimated less than 80% of section-2 which is close to 70% of section-2.

3.2 Timing Comparison

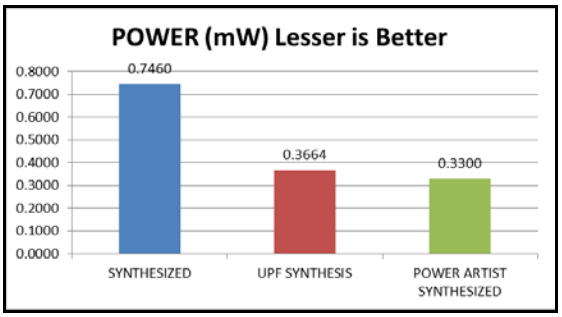

Fig. 7 RTL synthesis design Power comparison

- Since focus has been mainly on the power in this scope of study the timing will take lower priority but, it is must to have positive slack number during synthesis
- In all the four sections observed that the design has positive slack number

Section-2 RTL synthesized netlist with power management cells + UPF files has more slack that is because – power management cells uses low Vt cells which are faster compared to standard cells

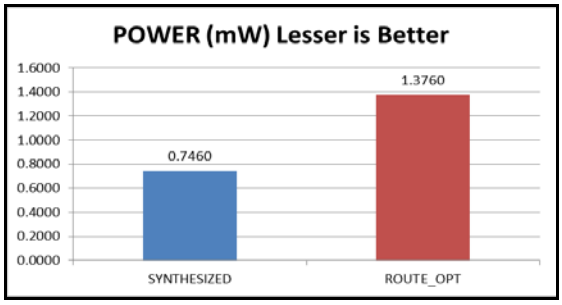

Fig. 8 RTL synthesis and PD Power comparison

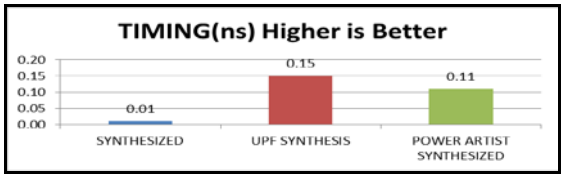

Fig. 9 Full system RTL design timing comparison

4. CONCLUSIONS

The goal of this study is to develop a highly correlated low power digital design flow with the Unified Power Format (UPF) standard incorporated. A detailed and elaborate explanation of the standard top-down based digital design flow has been presented. All the necessary stages a digital design has to go through post RTL development, i.e. synthesis, place and route, timing and verification has also been presented. Traditional methods to laying out digital circuits and design challenges associated with it with shrinking process technologies have also been discussed.

The metrics when devising a digital design flow being area, power and timing have been monitored at every stage in the flow. The flow is essentially a feedback loop that will go back in stages if the design performance output is not as expected. This iterative approach in developing digital design flow improves the correlation between the logic synthesis and the physical design stage. Existing design flows and physical design challenges associated have been discussed.

A top-down digital design flow for a flash based mixed signal microcontroller has been implemented. Also, a UPF synthesis flow for the same design has also been implemented. The design is constrained at a clock speed of 7ns. Results at every stage in the flow have been monitored for area, timing and power. The standard top-down flow has been implemented with 45nm technology to set up an initial complete flow and the low power design flow is implemented with a 45nm technology. Comparisons with the UPF implemented after synthesis has been explained. The UPF synthesis is implemented with two voltages, 1.2V and 0.9V and two sets of standard cell libraries that contain special cells required for the implementation.

Area, power and timing metrics have been compared with the low power flow. Power savings of about 20% have been achieved in the design flow with 'multi-threshold' power technique compared to that of the design flow with no low power techniques employed. A cumulative power savings of 51% has been achieved in a complete power efficient design flow with UPF synthesis.

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