Design and Development of Cost Effective Virtex-5 General Purpose Board

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Abstract

This study is aims towards development of cost effective Virtex-5 board which allows designers to experiment with features of Virtex-5 LX FPGAs at affordable cost. It has many advanced interfaces like Ethernet, System Ace, Platform flash Video Codec, optional user clock, Keyboard and Mouse interface etc., These interfaces are very much useful for industrial and consumer applications. But this makes the cost of the kit very expensive for students and amateur designers. Fundamental interfaces with which the experiments and most of the operations can be carried out would be very much sufficient for them.

Power plane split is carefully made considering potential EMI issues. DDR2 signals have been grouped together according to data, mask and strobe bits. These have been routed in group in layout as well. Signal Integrity and EMI analysis have been carried out to ensure good signal quality. For DDR2 signals over shoot and undershoot in voltage levels have been diagnosed and rectified. DDR2 signals have been length matched for precision of 25mil to attain good timing of the signals. Components have been selected based on RoHS compliance abiding to EU ROHS 2002/95/EC, Obsolescence, Lead-time, risk factors like Technology, Whisker and packaging. Layer stack-up for 12 layers have been built thereby providing excellent ground reference for all signals.

Overall cost of the newly designed cost effective Virtex-5 board design is reduced to nearly 50%. Peak emission remains at 37.7 dBuV/m. As a result of Signal Integrity analysis, 14 address lines, 16 Control signals, 64 data signals, 8 data mask signals and 16 strobe signals (8 pairs) which belong to DDR2 do not have issues due to reflection.

Key Words: Virtex-5 FPGA, Signal Integrity Analysis, Dual Data Rate (DDR2).

Nomenclature

BPI	Byte-wide Peripheral Interface
CPLD	Complex Programmable Logic Device
DDR	Dual Data Rate Memory
DFM	Design For Manufacturability
DIP	Dual Inline Package
EMI	Electro Magnetic Interference
EDA	Electronic Design Automation
EEPROM	Electrically Erasable Programmable ROM
HDL	Hardware Description Language
I2C	Inter Integrated Circuit
JTAG	Joint Test Action Group
LVPECL	Low Voltage Positive Emitter Coupled Logic
QFN	Quad Flat No Lead
SPI	Serial Peripheral Interface
SMT	Surface Mount Technology
CSP	Chip Scale Package
SERDES	Serializer / Deserializer
TTL	Transistor-Transistor-Logic
USB	Universal Serial Bus
ZBT	Zero Bus Turnaround

1. INTRODUCTION

Goal of this study is to develop cost effective Virtex-5 general purpose kit considering existing Xilinx ML501 Evaluation Platform as reference. ML501 is a wonderful kit which allows designers to experiment with features of Virtex-5 LX series FPGA. It has many advanced interfaces like Ethernet, System Ace, Platform flash Video Codec, optional user clock, Keyboard and Mouse interface etc., These interfaces are very much useful for industrial and consumer applications. This makes the cost of the kit nearly 990 USD [Avnet Express]. For students and amateur developers all of these interfaces may not be required. Fundamental interfaces with which the experiments and most of the operations can be carried out is very much sufficient.

### 1.1 Applications of Cost effective Virtex-5 General Purpose Board

This newly designed Cost effective Virtex-5 board is a great advantage for students and amateur design engineers. As this is general purpose kit, several applications can be developed using this kit. Using DSP present in FPGA, audio processing applications can be developed. Several audio processing algorithms can be implemented that compresses and decompresses digital audio data according to a given audio file format or streaming media audio format. The object of the algorithm is to represent the high-fidelity audio signal with minimum number of bits while retaining the quality. Typical uses of sound cards include providing the audio component for multimedia applications such as music composition, editing audio, presentation, education, games and video projection.

In addition to computer applications, DDR memories are widely used in other high-speed, memory demanding applications, such as graphic cards, which need to process a large amount of information in a very short time to achieve the best graphics processing efficiency. Video phones, storage devices and network connections are few more applications. DDR memory's primary advantage is the ability to fetch data on both rising and falling edge of a clock cycle, doubling the data rate for a given clock frequency. For example, in a DDR200 device, data transfer frequency is 200 MHz, but the bus speed is 100 MHz. DDR memory is well

suited for those designs that have a high read to write ratio. DDR memories can be used when interfacing with 32-bit microcontrollers and DSPs. Since many memories work with a 64-bit data bus, microcontrollers have to make a double data acquisition to get the less significant 32 bits first and then the more significant 32 bits. DDR memories have also been used to interface with FPGAs, giving those devices wide programming flexibility. FPGAs are often used to customize applications which combine many digital modules, such as a microcontroller with specific application hardware, USB controllers and printing modules. It is also common to find FPGAs used specifically as memory controllers to interface with other devices. DDR memories are suitable for these types of devices because they are fast and inexpensive compared with other RAM memories [Freescale].

2. Background Theory

Interfaces present in cost effective virtex-5 board design is as shown in Figure 1. DDR2 device from Micron which is 256MB 200pin. SODIMM has been interfaced. Memory organization is 32Meg x 64. DDR connector is right angle mount placed on the bottom side of the board. It has Xilinx LX series FPGA device, 676 pin count. 16x2 character display LCD is interfaced. Upon studying advantages of USB interface over Ethernet interface USB controller from Cypress CY7C67300 have been interfaced to FPGA. Crystal to LVDS clock Generator 25 MHz to 125 MHz is used. AC97 Audio codec with integrated headphone amp is used. IIC serial EEPROM of 8KBIT from ST Micro have been interfaced.
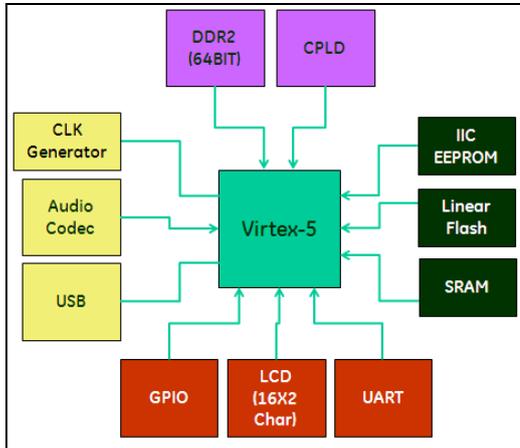
Fig. 1 Top level block diagram of Cost effective Virtex -5 board resolution.

Zero-bus turnaround SRAM with no bus latency of 256K x 36 from manufacturer ISSI has been interfaced. Each and every interface have been carefully analyzed and looked for opportunities to reduce cost. System interface, scratchpad memory, Ethernet interface have been removed. For many devices low cost component have been chosen which is equivalent in form fit and function. Based on literature survey, advantage of USB interface over Ethernet interface have been studied well and Implemented in cost effective Virtex-5 board design.

3. Circuit Design, Library and Schematic Capture

To start with design, engineer need to select appropriate components specific to application of circuit. Component should be selected based on 3 main factors:

1. RoHS compliance with proper documents preferably IPC-1752-2, as it is provides homogeneous level material declaration

2. Obsolescence - Only active components should be used. Obsolete or End-Of_Life announced parts will not be available in market to be sourced

3. Lead-time - Long lead time could hamper product cycle time

Fig. 2 Tin whiskers [Dr. Pietro Fontana, 2008]

Apart from these, components should be checked for other risk factors like Technology, Whisker and packaging. Selection of through hole components for lower voltage parts is a disadvantage as it affects the aspect ratio of the board. Aspect ratio of the board is defined as Ratio of circuit board thickness to the smallest hole diameter. And also, too many through hole components hampers good use of many signal layers. It makes routing unnecessarily difficult. And also, most of the components are built in SMT package. Some of the through hole packaging technology like DIP is old and most of the components which were available in DIP package earlier, are now available in small SMT packages. So, packages like DIP should be avoided. Components susceptible to tin-whisker growth should be avoided.

3.1 Library Development

Schematic symbols are the graphical representation of electrical/electronic components. It could be in ANSI format or in user defined format. Set of such graphical representations is called schematic symbol library. Sub libraries for actives components, passives, memory devices, connectors…etc., can be built. Many CAD tools have built-in symbol libraries. Land pattern on which electrical/electronic components sit on PCB is called footprint. Following are basic elements of footprints.
SMT Pad - This is a land pattern on which component can sit on PCB either on component side or on solder side. It cannot pass through different layers. Plated Through hole pad - This is for placement of through hole components. From this pad, electrical connections can be made on all layers. On power plane layers thermal spokes gets connected to these pads. Anti-pad takes care of the isolation inside power plane. The inside outline of this hole is coated with metal plating of generally 70 micron thickness. That is why the name

plated through. Non-Plated through hole pad - These holes do not have electrical connection. These are mainly for connector plastic pegs, tie holes, isolation slots etc. No plating is done inside the hole. In fact, padstack is built such a way that, pad is made smaller than drill, so that, accidental plating is avoided.

3.2 Detailed Block Diagram Development

Once top level block diagram is developed, instead of straight away jumping into detailed schematic design, developing detailed block diagram is very much necessary. This gives designer good grip over circuits being built. MAX3221 RS-232 block diagram. It consists of one line driver, one line receiver, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides electrical interface between an asynchronous communication controller and the serial-port connector. DDR2 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR2 SDRAM devices.
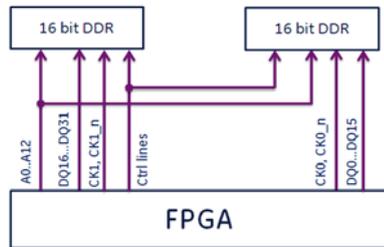

Fig. 3 DDR2 interface with FPGA

DDR2 SDRAM modules use DDR architecture to achieve high-speed operation. I²C uses only two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL), pulled up with resistors. VCC3V3 is the supply voltage connected to 3.3V. Typical voltages used are +5 V or +3.3 V although systems with other voltages are permitted. All Read, Write and Deselect cycles are initiated by the ADV input. A0 to A18 and D0 to D15 are address and data lines respectively. READ and WRITE are read/write ports as name suggests. CS is chip selects which enables the slave device. UB and LB are upper and lower byte signals. SRAM IS61LV51216 interfaces with FPGA. All Read, Write and Deselect cycles are initiated by the ADV input. A0 to A18 and D0 to D15 are address and data lines respectively. READ and WRITE are read/write ports as name suggests. CS is chip selects which enables the slave device. The FPGA, Platform Flash PROM, and CPLD can be configured through the JTAG port. The JTAG chain is also used to program the Platform Flash PROM and the CPLD. The configuration mode should be set to 101. The Super Clock module generates stable, low phase noise, 100Ω differentially terminated reference clock outputs utilizing a crystal-to-3.3V LVPECL frequency synthesizer from Integrated Device Technology. The dual-crystal interface provides a platform capable of supporting two selectable clock rate outputs with a voltage-controlled oscillator range of 490 MHz to 640 MHz. Control is provided through on-board switch

selection external board interface connector when connected to a host board. Power is supplied externally at 5V DC from a stand-alone supply, or optionally through the 1 x 32 external board interface connector, and is regulated on-board at 3.3V DC. EZ-Host has a general purpose 16-bit embedded RISC processor that runs at 48 MHz. EZ-Host requires a 12 MHz source for clocking. Either an external crystal or TTL level oscillator may be used. EZ-Host has an internal PLL that produces a 48 MHz internal clock from the 12 MHz source. EZ-Host has a built in 4K × 16 masked ROM and an 8K × 16 internal RAM. The masked ROM contains the EZ-Host BIOS. The internal RAM can be used for program code or data. EZ-Host provides 128 interrupt vectors. The first 48 vectors are hardware interrupts and the following 80 vectors are software interrupts. EZ-Host has two built in programmable timers and a watchdog timer. Input clock is 12MHz.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the cross point switch. A configurable sound engine provides enhanced record and playback processing to improve overall audio quality. The record path includes two digital stereo microphone inputs and an analog stereo input path. The analog inputs can be configured for either a pseudo differential or a single-ended stereo source. A dedicated analog beep input signal can be mixed into any output path. Audio codec is connected to FPGA. Description of each signal have been discussed earlier. MIC+/- are coming to microphone device. Input CLK frequency is 12MHz. SPP, SPN are differential signal going to buzzer. GPIO design provides a general purpose input/output interface to a Processor. Local Bus can be configured as either a single or a dual channel device.

Based on detailed block diagram, circuit diagram has been built. Circuit is hand written on paper. And it is built on bread board or other similar existing boards to test the functionality of the design. Once circuit functions as expected, then, it is translated to EDA tool. In the cost effective Virtex-5 board design, DX-Designer from Mentor Graphics is used for schematic capture. Captured schematics should be checked for Design Rule Check errors. Both electrical and other errors to be checked in schematics.

3.3 Layout Implementation

Board mount holes are basically Non-Plated holes placed at corners of the board. Sufficient clearance is provided to place washer. Copper/Brass stands can be placed on these corners so that, when assembled, board can be placed such a way that, components and wiring made in solder side do not get shorted. If the board is mounted on the slots/racks, copper/brass stand is not necessary. For Cost effective Virtex-5 board design, assumption is made that board will not be mounted on rack. In printed circuit board design, fiducial pads, also known as circuit pattern recognition marks, allow automated assembly equipment (also called as pick and place machine) to accurately locate and place parts on boards. These devices locate the footprint land pattern by providing common measurable points. Initial approximation of board dimension, 5.55 in X 5.43 in have been considered. Solder mask open is provided for 1mm width around the board edge. Figure 4 shows

board keep out areas. This helps in better isolation and it creates margin for PCB. This is very much necessary while handling the board. Route keep-in outline is mentioned. Thereby preventing component, route and copper being placed very close to board edge. Floor planning is about base plan for component placement on a printed circuit board. It depends on shape and size of the PCB, design flow in the circuit, mechanical and thermal constraints, product functionality requirements etc. Constraint driven methodology drives a good placement capability. The engineer or designer can assign components or sub circuits to specific "rooms" during design entry or floor planning. Components can be picked as per reference designator with help of netlist or BOM. Cost effective Virtex-5 board has 479 components. It needs precise placement management. As high-speed board requirements become more stringent, good plan for placement of critical components has become a necessity. PCB design is 90% placement and 10% routing.
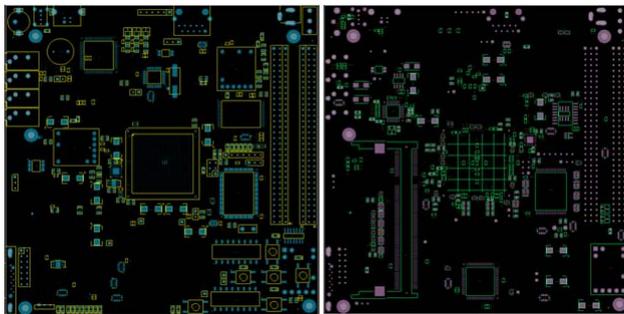

Fig. 4 Complete component placements

Component placement is most important aspect of board layout. Good component placement is key for easy layout work and gives best electrical performance. Lot of planning and paper work is required. Every engineer has different and best approach for placement. It is unique to each engineer. There is no hard and fast rule for component placement. However, by implementing certain good practices helps good electrical performance and ease of routing.

3.4 Layer Stack-Up

Performance of the PCB is greatly affected by layer stack-up. Inappropriate materials and poorly designed substrate also reduces electrical performance and signal transmission as a result of increase in emissions and cross-talk. It also increases tendency of product absorbing external noise. This in turn increases timing glitches and interference affecting products performance. In the long run, it affects confidence and reliability factors. On the other hand, good substrate reduces electromagnetic emissions and cross-talk. By providing low inductance power distribution network, it improves signal integrity. It also improves manufacturability of the product. Preventing factors which affects board performance is better than trying to solve errors/problems later on. PCBs with sufficient power planes enable signals to be routed either in micro strip or in strip line. Thereby, creating less radiation. Multi-layer PCB has additional advantage over 2 layer board in terms of low radiated emission[Henry W. Ott, 2000]. Following factors should be considered while building multilayer stack-up. One of the most commonly used Dielectric materials is FR4. Could be

used as core or pre-impregnated material. The pre-peg material is thin sheet of fiber glass impregnated with uncured epoxy resin which hardens when heated and pressed during the PCB fabrication process. Minimum pitch of SMT component, BGA ball counts, clearances, and via dimensions are few factors which determines layer count. Once these rules have been established, calculate the stickup required for the desired characteristic impedance (Zo) and the differential impedance (Zdiff) as per the component datasheets. Generally, 50 ohm Zo and 100 ohm Zdiff are used. Lower impedance will increase the dI/dt and increases current drawn. Higher impedance increases EMI emission and makes design susceptible to outside interference.

4. CONSTRAINTS

A physical constraint takes care of rules mentioned on Line width, via types, routing layers specific to net names. General minimum line width considered is 5 mils (0.127mm) and maximum is 125 mils (3.175mm). Although general tracks are not 100mils+ width, that is the margin applied. For supply and ground signals, trace width is much bigger (0.254mm). For signals inside FPGAs, constraints are set considering air gap between BGA balls. For differential pairs spacing between each signal ended stranded is defined with tolerance. Neck gap is set to 0.1524mm. Spacing constraint is about clearance among Line to line, via to line, pin to via and same With respect to same net. Constraints have been set for line, SMD pin, through hole pin, shape, via and NPTH holes. Maximum uncoupled length is 6mm. This is a real challenge to achieve in such a complex board and tolerance of 0.245mm. There is tight tolerance of 0.01mm. Dcap supplies required power in when placed in shortest possible distance. If supplied path impedance is large, it becomes a source of radiation due to switching noise. More than 2 decaps connections should not be routed to one via. Supply, ground trace must be as short as possible. Decaps must be placed on same side as much as possible. Decap route of one device should not be mixed with supply and ground traces from other sources. Series terminations remove reflection at the clock source. The main advantages of Series termination is, it is very simple to implement. Precise value at precise distance plays key role. Consumes very less power. Acts as current limiter while driving high capacitive loads. Improves jitter performance by ground bounce reduction.

5. CRTICAL SIGNAL ROUTING

DDR2 memory module is high-speed, CMOS dynamic random access memory module. DDR2 SDRAM modules use DDR architecture to achieve high-speed operation. DDR2 architecture is essentially a 4n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins [Altera]. DDR Signals can be grouped as following:

- Clocks signals

- Data bus

- Address bus
- Control signals

All DDR clock pairs should be routed in same layer. Daisy chain topology should be maintained for data signals routing. Solid ground reference plane should be maintained for all DDR signal routing. When routing the byte lanes, signals within the same byte lane should be routed on the same critical layer. Series damping resistor placement should be as close to the first DIMM as possible. Discrete component placement should be optimized in favour of data bus. Individual data bits across different byte lanes should not be swapped. DDR signals should be properly grouped bits wise. 8 data line bits, 1 data mask bit and data strobe bit. Yellow highlighted routes in Figure 5 shows DDR signal routing.
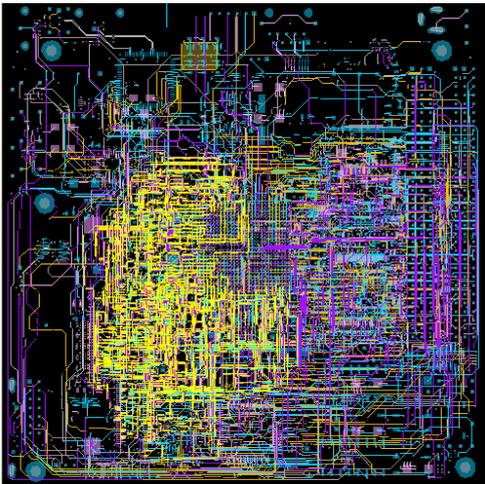

Fig. 5 PFD Implementation and it waveform

6. RESULTS AND DISCUSSION

When signal affects nearby signal due to capacitive or inductive coupling it is called cross talk. This un-intended interference is called noise. Traces have to be sufficiently isolated and solid ground plane have been provided to get rid of these noises. In printed circuit boards, a trace with its reference plane constitutes a type of transmission line. Pair of parallel conducting wires separated by a uniform distance, such as the pins, wires in a cable or socket and via are transmission lines [Eric Bogatin]. All the transmission lines have basic parameters such as a) per-unit-length resistance b) Inductance c) Conductance d) Capacitance e) Unit-length time delay f) Characteristic impedance. As models for many interconnects can be treated as transmission lines, understanding basics of transmission line theory is necessary. Familiarity with common transmission line effects in high-speed design is also required. Reflection noise increases time delay and causes overshoot, undershoot and ringing. Impedance discontinuity along the signal transmission path cause reflection noise. When a signal changes its routing layer and impedance values are not consistent, reflection will occur at the discontinuity boundary. When a trace is routed over planes with perforations at different locations, crossing a gap, having branches, or passing the proximity of another trace, impedance discontinuity will occur and reflection can be observed. When a signal finally reaches the receiving end of a

transmission line, if the load is not matched with the transmission line characteristic impedance, reflection will also happen. To minimize reflection noise, common practices include:

- Controlling trace characteristic impedance
- Choosing appropriate termination scheme
- Using a solid metal plane as the reference for return current.

Cross-talk impacts timing on the active lines if multiple lines are switching simultaneously. The amount of cross-talk is related to a)Signal rise timem b)Spacing between the lines, and to how long these multiple lines run parallel to each other. To control the cross-talk, one can make the lines space apart, add ground guarding band in between the signal lines, keep the parallelism to minimum, and keep the traces close to the reference metal planes.

6.1 Problems Diagnosed by SI Analysis

Timing and quality of the signal is addressed by SI analysis. The time when signal reaches its destination and quality of signal at that point of time is of significance. Ensuring reliable high speed data transmission is the objective of SI analysis[Douglas Brooks]. Transmission of signals happens from one component to another in the form of logic low or logic high. VIH is voltage above reference voltage. It is considered as logic high. Voltage below reference voltage is VIL (logic low). Receiver device samples waveform thereby encoding binary information. Data is sampled either at rising edge or at falling edge of clock. Data must arrive at the receiving gate at right time and settle down to a non-ambiguous logic state when the receiving component starts to latch data. Data transmission is hampered by any delay in data arrival time or distortion of waveform. Timing factor is dependent on delay caused by trace length where signal propagates. Three major factors causes waveform distortion.

- Reflection Noise – Caused by impedance mismatch, stubs, via and other interconnect discontinuities
- Cross-talk Noise - Caused by electromagnetic coupling between signal traces
- Power/Ground Noise – Caused by parasitic effects of power/ground delivery system during drivers' simultaneous switching output. This is called Ground Bounce

Other factors like EMI/EMC causes signal distortion. When these problems occur and system noise margin requirements are not satisfied, input to a switching receiver varies below VIH or above VIL. This disturbs data being latched causing logic error. These types of faults are quite difficult to diagnose once system is built. So, preventing occurrence of these problems is essential.

6.2 Impact of SI Analysis

The trace passes through various interconnects like pad, via, copper etc. Along the path any impact at source-end or receiving-end affects signal in terms of time and quality. SI Analysis is not a newly invented technology. In recent time there has been tremendous increase in user requirement. As people and systems like military,

medical and aerospace need connectivity at all times through high-speed digital communication/computing systems, expectation over quality of digital systems and signals has increased largely. SI Analysis plays crucial role in guaranteeing reliable operation of these systems. Without SI analysis, products fail in field. Guidelines developed at this stage are applied as constraints in design for component placement and routing. Once placement and routing is completed based on these constraints, violations such as reflection, noise, ringing, cross-talk and ground bounces are checked for correctness. When post route SI analysis is done, assessment can be made on real tracks and components instead of estimated data and models. So, with post route SI analysis, reliable high performance of the system can be achieved with good turn-around time. In order to achieve this, engineers are required to analyse electrical characterization of the technology from signal integrity point of view and there by develop guidelines for layout. Engineers use SI modeling and simulation software. These SI tools must be accurate and efficient to model individual interconnections such as via, traces, and power/ground plane stack-up. SI analysis should be carried out for few critical nets. For cost effective Virtex-5 design, SI analysis have been carried out for DDR signals. Input/output Buffer Information Specification is used to describe the analog behavior of the input and output. IBIS models can be procured from device manufacturers. With IBIS models, simulation tool vendors can accurately model compatible buffers in SI simulations. These models are capable of maintaining accuracy and speed in simulation of transmission lines and signal integrity related effects such as cross-talk. A behavioral device model exposes proprietary information about design technology and the underlying fabrication processes. Behavioral IBIS models provide DC current vs. voltage curves.

For cost effective Virtex-5 board design most of the IBIS models have been found in manufacturer's website. These models have been added to Allegro SI analysis tool and extracted topology in cadence SigXplorer tool. Figure 6 and 7 shows the SI Analysis results obtained for DDR2 address lines:
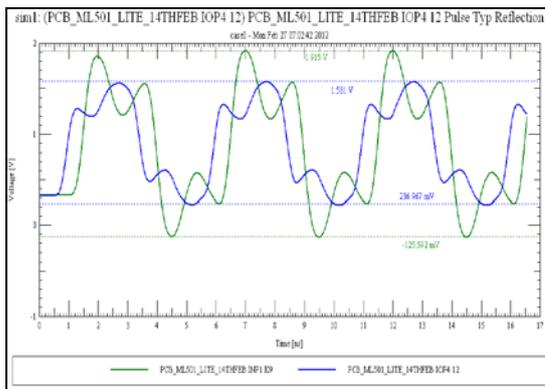
Fig. 6 DDR2_ODT signal having lot of noise
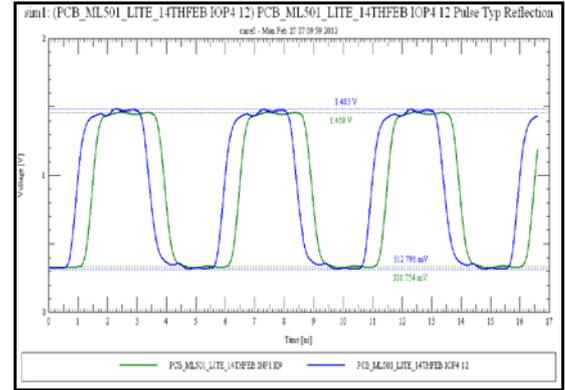
Fig. 7 DDR2_ODT no noise after termination position change

When waveforms are distorted, termination is moved closer to DDR2 device with appropriate termination value. And resulting waveform shows significant improvement in signal quality. Shunt termination of 50 Ohms and supply voltage of 0.9 V have been used as it has to be half of the actual voltage. IBIS model of DDR2 device is used. Due to difficulty in obtaining IBIS model for DDR2 slot, IBIS model for DDR2 device have been used for performing SI analysis on Cost effective Virtex-5 general purpose board design.

7. CONCLUSIONS

As a result of extensive literature survey made many guideline and best practices have been incorporated in Cost Effective Virtex – 5 general purpose board design. Effort have been made to reduce cost in many aspects: a) In terms of retaining most required interfaces without reducing function of the board b) in terms of reducing board dimention c) In terms of selecting low cost components which is equivalent in form fit and function. Careful attention have been given for DDR2 routing and building layer stack-up. IPC standard have been followed for building footprints. Industry standard guidelines have been followed in schematic diagram capture. DDR2 guidelines and publications have been followed for length matching signals. Design Constraints have been set as per DDR2 guidelines. SI analysis and EMI analysis have been performed and ensured good signal quality. Power plane splitting is done meticulously so as to get good EMI performance. Several DFM guidelines have been followed for better yield of the board. Artwork files have been generated for all layers. Newly designed kit "Cost Effective Virtex-5 General Purpose Board" cost nearly 50% less compared to existing product.

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