Design and Implementation of Frequency Lock Loop for High End Task Processor

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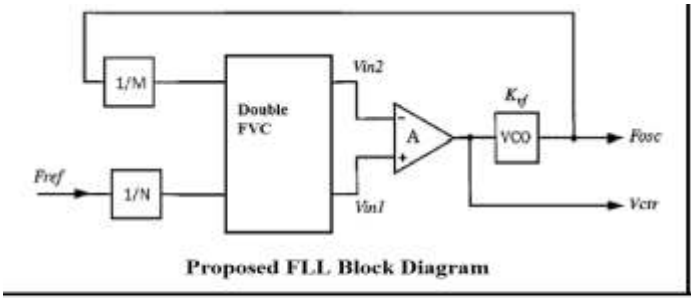
Keywords: FLL, Clock Lock Loop, Jitter, GHz, Low Power

Abstract:

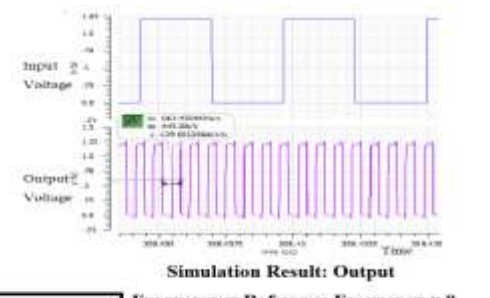
Task processing is the next generation of processing where the system comprises of a host processor and many slave processors or processing modules. The clock for each processing module is supplied from the host, low frequency clock is sent to avoid losses, which can be multiplied at the slave unit. Serial communication protocols have grown to support this growth in processing. Serial communication protocols works with a secondary clock unrelated to the master clock, eliminating the need for task processor to work in sync with host processor. Phase Lock Loops (PLL) are widely used for clock multiplication today, but are associated with limitations like high leakage power and high jitter. These limitations are due to the loop filter in the circuit, which has a huge capacitor leading to high leakage also disturbing the jitter performance.

The aim of the work is to design and implement a Frequency Lock Loop (FLL) for high end task processors. FLL is proposed as the clock locking loop to overcome high leakage power and high jitter limitations of PLL. Architecture for each sub-block of FLL has been selected and designed with low power and low jitter as target. The top level loop integration, simulation and characterization of the design have been carried out. Corner simulation has also been performed to ensure manufacture-ability and better yield. The schematic design of FLL has been transformed into layout and parasitic simulations are also performed.

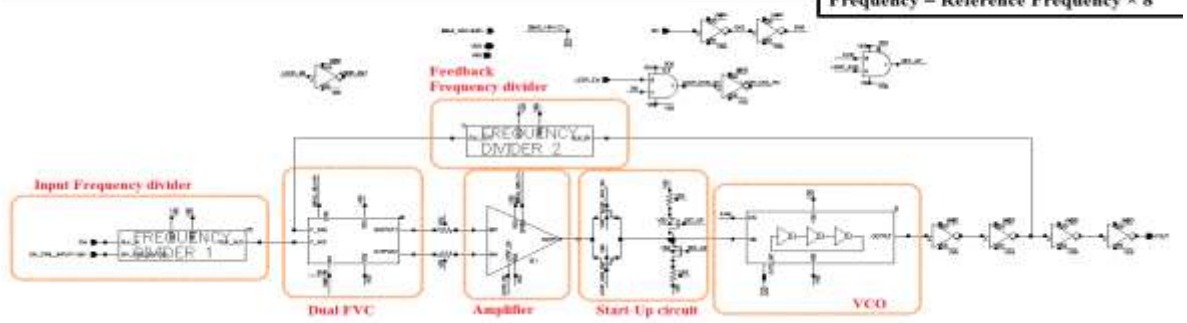
The clock for a task processor of 500-1500 MHz is generated using FLL. FLL has been designed for the aligned specifications occupying an area of 0.411 sq.µm. Simulation results show that the peak jitter is 6 ps. The circuit consumes a peak current of 2.9 mA, and the average current stands at 1.03 mA. This gets the average power consumption to 1.236 mW. Hence, the designed FLL is a suitable block for clock multiplication in task processing applications.



Proposed FLL Block Diagram



Simulation Result: Output Frequency = Reference Frequency × 8



FLL schematic