Design of Ultra Low Drop Out Regulator for Audio Devices

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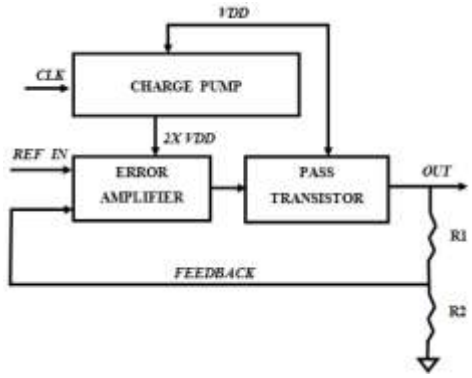
Abstract:

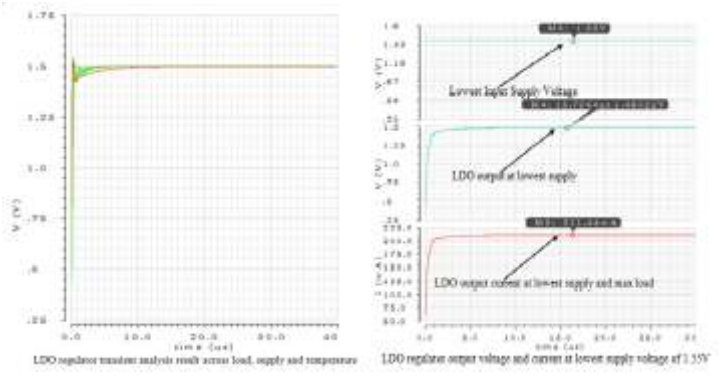
Low Drop Out (LDO) Regulators are widely used in battery-powered portable electronic devices because of their low dropout, low quiescent current and large load current characteristics with minimum heat losses. LDO regulator is used to power up analog blocks to improve the Power Supply Rejection Ratio (PSRR). Ultra-low drop out improves the supply voltage margin. PMOS LDO regulator needs large on board compensation capacitor for stability at no load due to several poles embedded in the loop. Use of NMOS LDO regulator topology enables internal compensation by eliminating the need of large on board capacitors, saving area and cost.

In this work, the proposed NMOS LDO regulator uses a telescopic error amplifier topology and single stage charge pump with non over lapping clock logic. The telescopic cascode error amplifier topology with NMOS pass element output stage will increase the PSRR of the LDO regulator and also reduces the area by using internal compensation. The non over lapping clock logic minimized the charge pump losses enabling ultra-low drop out. The schematics design of ultra-low dropout regulator has been developed and analyzed its performance against specifications. Pre and Post layout simulations have been carried out to ensure functionality and performance with parasitic. The design has been implemented in 180 nm CMOS technology.

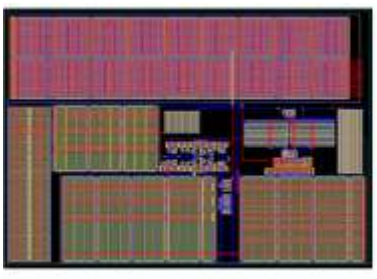
The experimental result shows the proposed ultra-low drop out regulator is able to deliver 1.5 V regulated output with 200mA load current over supply voltage range of 1.95 V to 1.55 V with a bandwidth of 20 kHz. The drop out voltage is only 50 mV at max load current (200 mA) for minimum supply. Load regulation is 0.1 mV/mA and line regulation is 1 mV/100mV. The LDO regulator has a PSRR of -56 dB at 20 kHz. The area of the low drop out regulator is 0.1 mm^2.

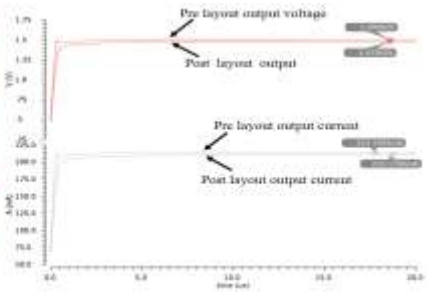


Block diagram of proposed ultra low drop out regulator



Proposed LDO regulator transient analysis result





Layout implementation and post layout simulation of proposed LDO regulator