Design and Implementation of Scan Chain Architecture for Reducing Test Power and Time

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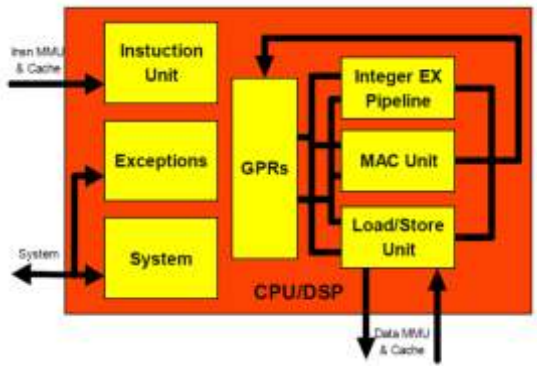
Abstract:

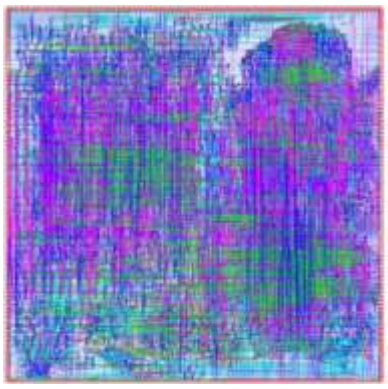
In the deep sub-micron technology, devices are shrunk to nano meter scale. Variations in manufacturing processes lead to defect in the silicon chips. Scan chain testing technique is used to isolate the defective silicon chips and eliminate them before shipping to customer. In the lower technology node, number of gates fabricated on silicon chips increases and it leads to higher power dissipation in the silicon during functional mode and as well as testing mode. During exhaustive testing all the gates in a silicon chip are activated which creates hot spot and it leads to temporary or permanent damages in the silicon chip. Higher gate count also leads to higher test time which in turn increases the test cost. Use of parallel scan chain with two enable signal in the scan chain reduces both the test power and time.

In this work, the proposed scan chain architecture uses parallel scan chain with two different enable signal. Parallel scan chain will reduce the number of flip-flop active in a given instance. The proposed technique is to providing two different enable signals for parallel scan chain, testing can be done for the first 50% of silicon and if defects are found, silicon can be dropped without testing remaining 50% of silicon. To implement this technique open core processor OR1200 is chosen and it is implemented in 65 nm TSMC process. OR1200 is a 32bit Reduced Instruction Set Computer (RISC) with Harvard architecture processor.

The experimental results shows that the proposed parallel scan chain architecture with two different scan enable reduced 20% of test power and 18% of test time. Test power is reduced from 925 µW to 728 µW. Test time is reduced from 506 µs to 401 µs. The silicon area is increased due to additional logic gate from 36156.76 µm² to 40231.2 µm².



Or1200 Units



Or1200 Layout

	Initial Design	Proposed Design
Test Power	925 mW	728 mW
Test Time	506 µs	401 µs

ATPG Results of OR12