Optimisation of Timing and Power of High Frequency Functional Block in Deep-Submicron Technology

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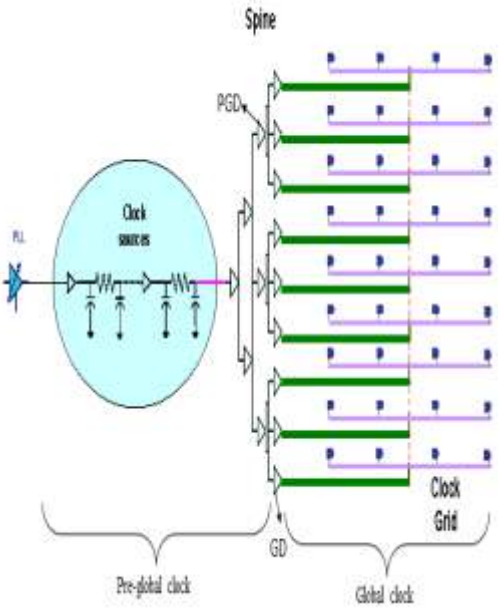
Keywords: Physical Synthesis, Power Optimisation, Clock Network, Leakage Power, ASIC

Abstract:

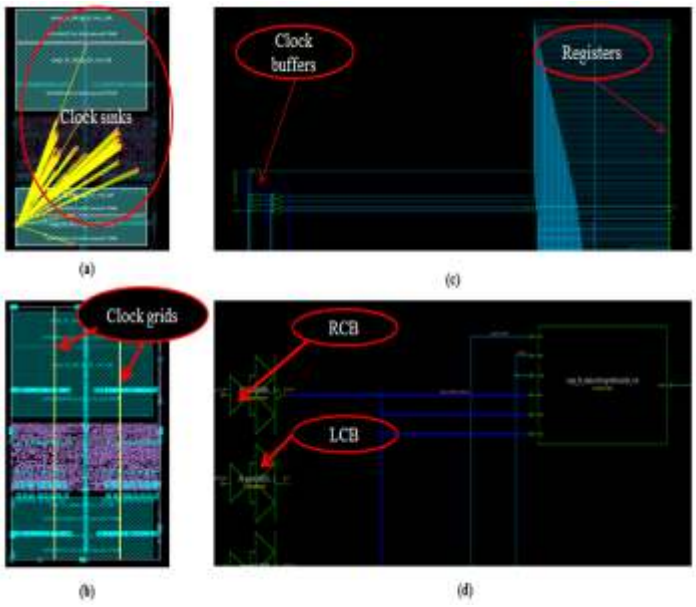
Although ASIC design methodology has been used for more than thirty years, today's designers working with deep submicron technology face a new set of technical challenges. Because of the increasing burden of the over design necessary to meet strong timing guarantees, power requirements and design flows need to be aware of the more subtle effects of particular design. Recent studies have shown the effectiveness of applying existed Physical Synthesis methods, multi-bit flip-flops and clock gating techniques to save the power consumption of the clock network. However, all the previous works applied these techniques at corresponding design stages, which could be very difficult to carry out the trade-off among power, timing, and other design objectives.

This project presents a power-aware placement method that simultaneously performs (1) activity-based register clustering that reduces clock power by placing registers in the same leaf cluster of the clock trees in a smaller area and (2) activity-based net weighting that reduces net switching power by assigning a combination of activity and timing weights to the nets with higher switching rates or more critical timing. Novel power optimization methods by incrementally applying vectoring at the post-placement stage and RCB/LCB clock enable methodology at the CTS stage to gain more clock power saving while considering the placement density and timing slack constraints, and simultaneously minimizing interconnecting wire length.

One of the functional digital block "sbblds" which has 6000 cells and input frequency 5.4 GHz in the SoC is implemented by these modified design flow and new techniques in the 14 nm technology. The maximum and minimum timing is improved from -157 ps and -54 ps to zero. The number of sequential cells is reduced from 1143 to 965 because of multi bit flip-flops. The number of buffers also reduced from 1202 to 1153 due to effective clock tree RCB/LCB structure. Switching power is reduced from 55.94 µW to 19.32 µW and it's almost 60% improvement. The leakage power also reduced from 1.3 µW to 0.7 µW and it's almost 45% improvement in leakage power.



Optimised clock distribution network



(a) Clock sinks before CTS, (b) Clock meshes (clock-grids), (c) Clock buffer tree, (d) RCB/LCB buffer structure