Design and Analysis of Phase Frequency Detector and Charge Pump for Low Phase Noise PLL

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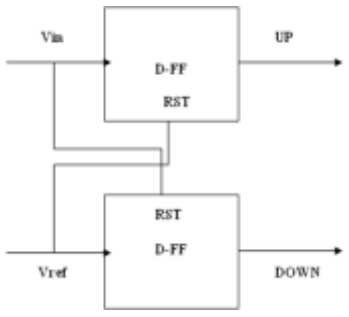
Abstract:

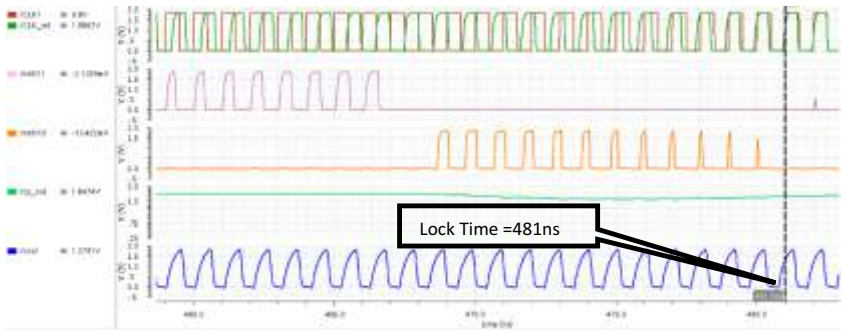
Phase Locked Loop (PLL) are employed in communication system for clock synthesis, synchronization and skew reduction. Phase noise or jitter is one of the important performance parameter which is not desirable in Radio Frequency (RF) communication since it corrupts the carrier signal and it results data degradation. Practically, phase noise of PLL cannot be removed completely, but it can be possibly minimized by proper design of its sub blocks. This thesis presents design and analysis of PLL. The PLL design consists of low power phase and frequency detector, low jitter charge pump, second order loop filter and five stage current starved ring oscillator.

In this work, clock-reset PFD architecture has been proposed which reduces the effects of dead-zone and consumes less power when compared with other architectures namely AND, NAND and NOR based PFD of Phase Frequency Detector (PFD). A second order loop filter which minimizes the spurs level and a voltage controlled oscillator is designed to match the input frequency. Single ended charge pump is employed in this circuit which has a current mismatch of 3.66% and producing 500 µA current at the pump output. Current starved ring oscillator acts as the Voltage Controlled Oscillator (VCO) which is designed to produce a 1 GHz output which has a gain of 713 MHz.

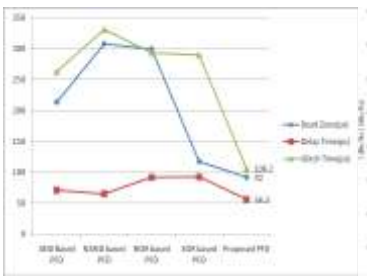
The PLL employing with the proposed clock-reset PFD has a capture range of ±100 MHz with a lock range of 481 ns. At an operating temperature of 27°, the phase noise imparted by the PLL to the carrier frequency is -135.1815 dBc/Hz whereas the phase noise imparted by the AND based PLL is -133.956 dBc/Hz. The PLL operates to produce 1 GHz oscillation and the average power consumption is 3.135 mW.



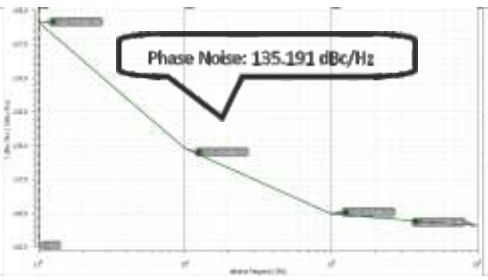
Proposed PFD



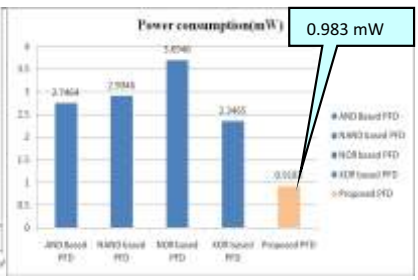
PLL in locked state



Comparison of PFD architectures



Phase noise of PLL



Power consumption comparison