# Design and Implementation of Low Power Floating Point Architecture in ASIC

| | | |
|---|---|---|
| **Student's Name** | **Kamarapu Sandeep** | **VLSI (FT-2012)** |
| **Academic Supervisor(s)** | Abdul Imran Rasheed | |
| **Industrial Supervisor(s)** | | |

**Kamarapu Sandeep**
sandeepkamarapu@gmail.com
Ph. No: 0 78294 29636

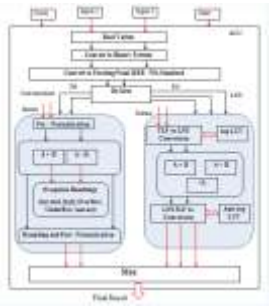
**Keywords:** Conventional Floating Point, LNS, FPU, ASIC

**Abstract:**

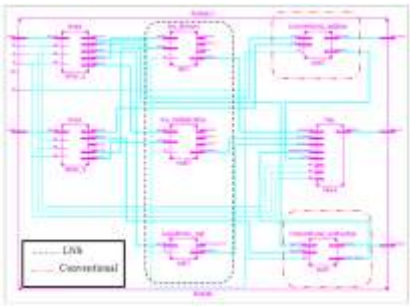
Floating Point Unit (FPU) is a math coprocessor which is specially designed to carry out the operations like addition, subtraction, multiplication and division. The main importance of floating-point representation over fixed-point representation is that, it can support a wider range of values with relative accuracy. It is used in applications such as communication satellites, music synthesizers, avionics, and graphics workstations.

Conventional and Logarithmic Number System (LNS) are two different types of floating point architectures which are available. In the conventional single precision floating point architecture, there are two optimization blocks namely pre-normalization and post-normalization blocks which are used to achieve better accuracy. The main drawback of this architecture is power consumption typically 1820 µW. Multipliers and dividers are the high power consumption blocks. In LNS architecture incorporation of single precision FPU for logarithmic and anti-logarithmic blocks, will reduce the power consumption. Usage of addition and subtraction blocks is the main cause of high power consumption. Proposed idea is to develop architecture of floating point unit for low power consumption. The design will incorporate both conventional and logarithm types of floating point units to overcome power consumption problems in both the architectures.

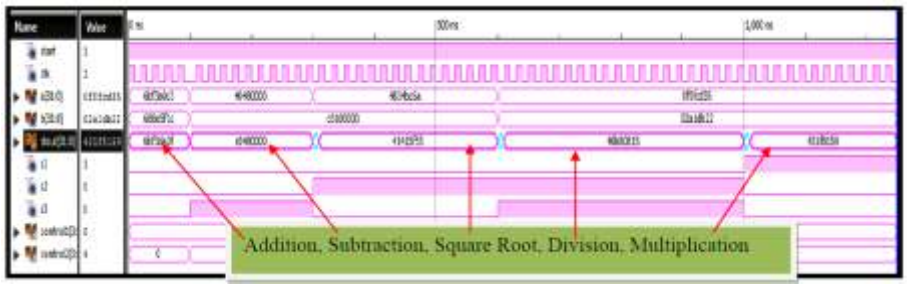
An integrated floating point Register Transfer Logic (RTL) architecture has been developed to achieve the high performance with low power consumption. For 65 nm technology the power consumption is 470 µW (five operations) at operating frequency of 240 MHz has been achieved. Comparisons shows that integrated conventional and LNS are more suitable for floating point technique with low power. RTL design of proposed low power floating point architecture requires minimum time delay of 7.782 ns, in comparison with conventional and LNS architectures.



**Proposed low power floating point architecture**



**Top level RTL architecture of proposed low power floating point architecture**




**Proposed floating point ALU test bench results**