Design and Analysis of Leakage Current Reduction Technique for CMOS Circuits

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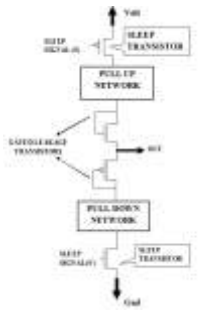
Abstract:

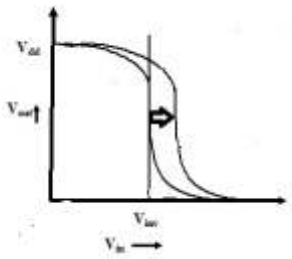
With the advent of Complementary Metal Oxide Semiconductor (CMOS) technology, scaling, transistor density as well as performance parameters of Integrated Circuits (IC) have been enhanced over the decades. But as the CMOS technology scales down further into the deep submicron regime, transistor supply voltage is scaled down. In order to maintain high drive current of the transistor, the sub-threshold voltage is also scaled down. Scaling of transistor sub-threshold voltage has resulted in drastic increase of sub-threshold leakage current which is a prominent issue in deep sub micron regime and many researchers have proposed various leakage current reduction techniques from the device level to the architectural level.

In this work, a novel leakage current reduction technique has been proposed by combing sleep transistor and GALEOR current reduction techniques. The proposed leakage current reduction technique has been designed and analyzed for sub-threshold leakage current at 180 nm, 90 nm and 45 nm technology nodes for CMOS logic circuits such as inverter, NAND gate and full adder. The existing sub-threshold leakage current reduction techniques namely stack forcing, sleep transistor, sleepy stack and GALEOR methods are also designed, analyzed and compared with the proposed sub-threshold leakage current reduction technique.

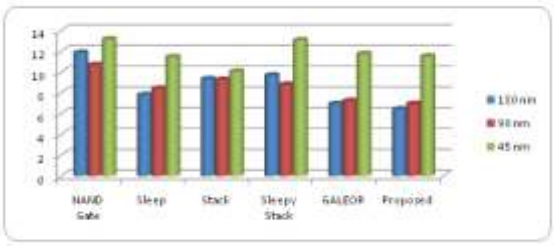
The simulation results shows that the proposed sub-threshold leakage current reduction technique provides 8% reduction in dynamic power and 21% reduction in static power when compared to other leakage reduction techniques. Further, the impact of scaling on leakage power is analyzed and observed. It is found that the proposed leakage current reduction technique holds well for 45 nm and above technology nodes.



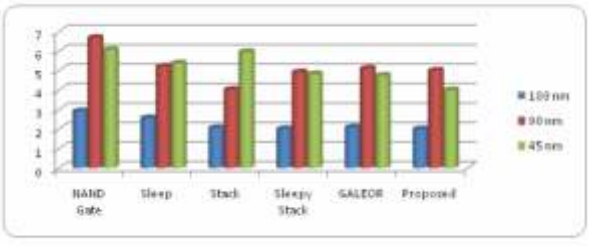
Structure of proposed leakage current reduction technique



Threshold voltage plot of 2 input NAND gate



Dynamic power results of 2 input NAND gate



Static power results of 2 input NAND gate