

## Design and Performance Analysis of a Folded Cascode Operational Amplifier



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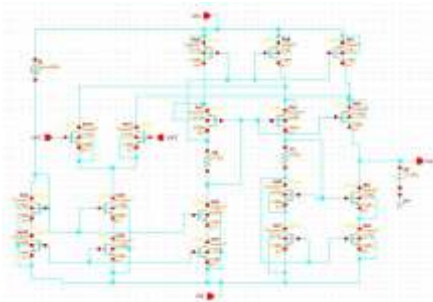
**Keywords:** Folded Cascode Op-Amp, Self-Biasing Technique, EMI

**Abstract:**

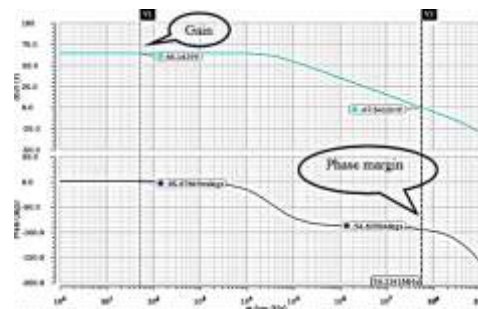
The increasing demand for high-resolution ADCs and DACs, voltage references, and sample-and-hold circuits have forced designers to propose novel high-speed and high-gain Op-Amps. To design high-gain Op-Amps with large bandwidth in low-voltage processes, innovative circuit design techniques are required. Folded cascode operational amplifiers are better choice for high gain op-amps and high speed applications.

This project work targets DC gain enhancement for folded cascode amplifiers. A modified design technique has been proposed for folded cascode operational amplifier using self bias technique to enhance the DC gain. In this architecture, simple current mirror of the biasing circuit is replaced by a cascode current mirror. This self biasing technique improves the output resistance of cascode current mirror circuit. The area of this architecture is reduced by avoiding complex external bias circuits.

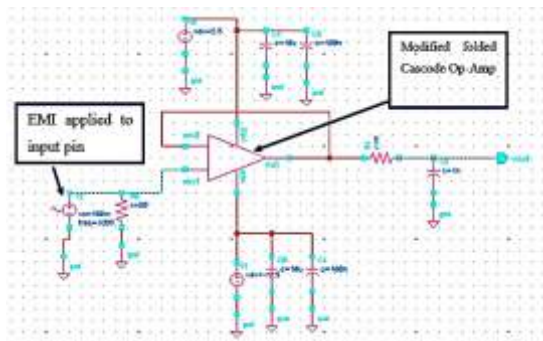
The simulation results have shown that the DC gain of folded cascode op-amp in 180 nm CMOS technology has achieved 64.143 dB and phase margin 85.316 degrees. The requirement of electromagnetic interference of op-amp for RF application is also measured. The voltage follower configuration test setup has been built to measure the DC offset caused by EMI effects. The DC offset of EMI effects are measured as minimum of 0.32 mV and maximum of 2.85 mV for 1 kHz and 1GHz respectively.



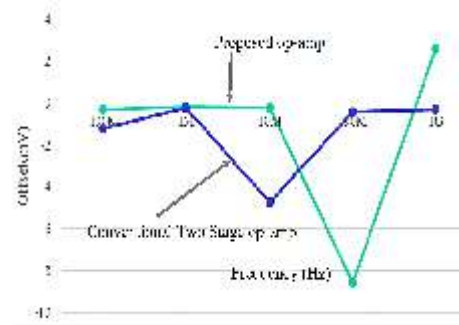
**Schematic of modified folded cascode Op-Amp**



**AC analysis of modified folded cascode Op-Amp**



**Test set-up to measure EMI applied to input pin**



**Comparison result of EMI applied to input pin**