Design and Implementation of WDF for Digital Down Converter on FPGA for LTE Application

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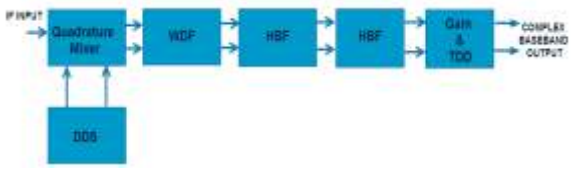
Abstract:

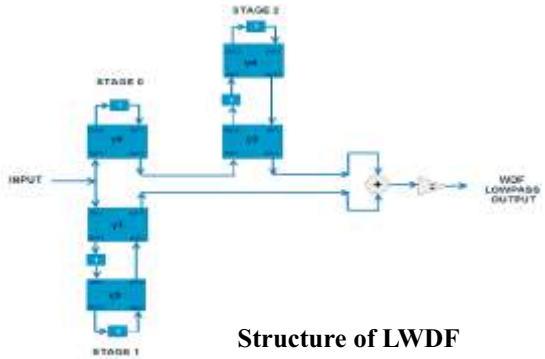
Tremendous growth in technology could be witnessed in various industrial and domestic applications. In particular internet and wireless communication networks are backbone for several systems. Wireless data traffic grows 66% a year which demands high speed data transmission and multimedia services. Development of highly efficient Digital Down Converter (DDC) is important to meet the growing demand for high speed communication. Chain of decimation filters can be used to perform channel filtering and decimation operation. Digital IIR filter known as Wave Digital Filter (WDF) is used as decimator as it offers guaranteed stability, low passband sensitivity, regular structure and also lower order to meet the desired filter specifications. This project focuses on design and development of WDF model and arrives at a modified DDC architecture suitable for Long Term Evolution (LTE) application.

The WDF are modelled by using the multiplier and alpha coefficient values which are derived using explicit formulas. Lattice WDF (LWDF) structure is chosen and the model is realized using Simulink blocks and incorporated as Xilinx black box. The designed LWDF is implemented as first stage decimator in the DDC system to perform decimation by factor of 2. For realizing the delay on hardware, RTL architecture of the modified DDC system has been developed and functionality has been verified.

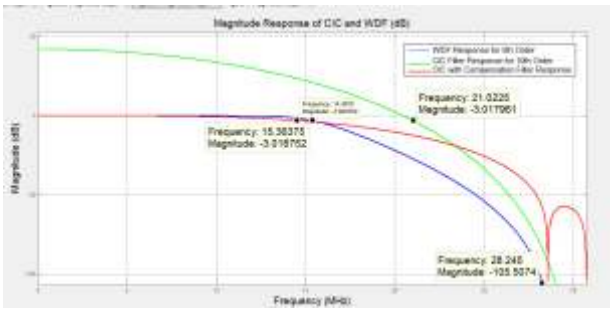
Functional simulation of LWDF, modified DDC system has been carried out and it is observed that the design takes 48 clock cycles to give a throughput of 7.68 MSPS. The RTL design of WDF based DDC for down converting 5 MHz bandwidth IF signal of sampling frequency 122.88 MSPS to 7.68 MSPS has been prototyped on xc5vlx110t-2ff1136 Virtex-5 FPGA. The proposed DDC design has utilized 422 slices, 1192 flip-flops, 11 DSP48Es, 1 Block RAM and 1035 logic cells on FPGA hardware thus resulting in overall less resource utilization due to the implementation of WDF and works at a speed of 140 MHz thus making it suitable for LTE application both in terms of area and speed.



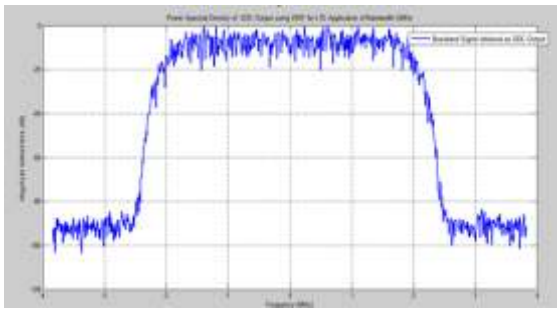
Block diagram of proposed DDC system



Structure of LWDF



Lowpass filter response of LWDF and CIC filter



PSD of DDC baseband output