Design and Implementation of Self Oscillating Sigma Delta Modulator

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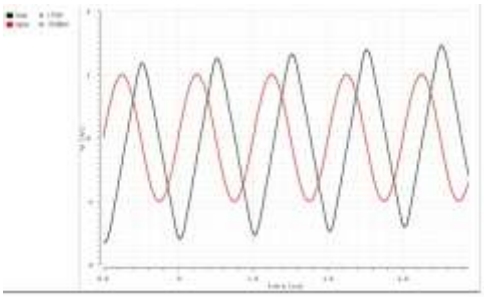
Abstract:

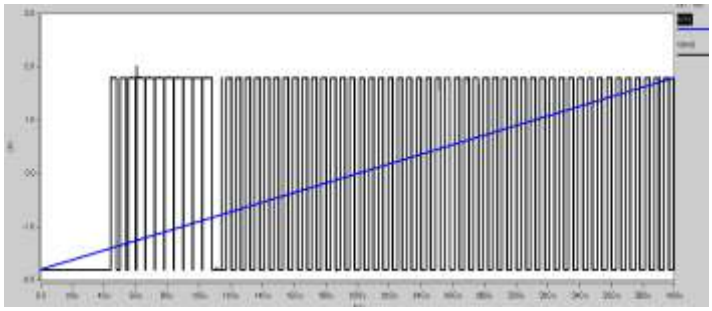
Analog-to-Digital Converters (ADC) play an essential role in design of modern communication systems. Oversampling converters like Sigma Delta Converters can be implemented using simple and high-tolerance analog components. The Sigma Delta Modulator (SDM) also provides the technique of noise shaping in addition to oversampling to achieve a high-resolution conversion. The advantage of Sigma Delta Converter is that the analog signal can be converted to a bit stream using a 1-bit comparator. Continuous Time Sigma Delta Modulators are the most commonly used to reduce power consumption of high resolution ADCs.

This project work deals with the design of first order self-oscillating SDM. The power hungry multi-bit flash ADC of the SDM is replaced by Pulse Width Modulation (PWM) mechanism. The advantage of using PWM mechanism is to eliminate the need of multi-bit Digital to Analog Converter (DAC), therefore making the circuit free from non-linearities caused due to the use of multi-bit DAC. Although PWM uses one bit quantization, the output is a lossless representation of its input. The Sigma Delta Modulator shows a self-oscillation property that provides the system to be independent of external clock frequency.

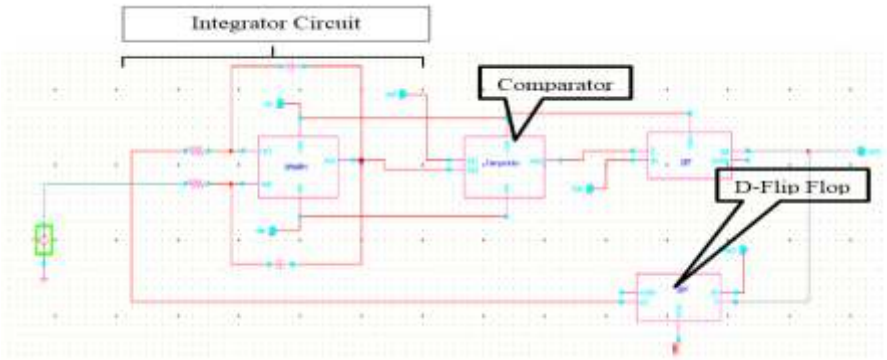
The simulation results have shown that the operational amplifier used in the first order sigma delta modulator has DC gain of 72.486 dB, phase margin of 52.7 degrees and a gain bandwidth of 8.0346 MHz. The self-oscillating Sigma Delta Modulator operates at a sampling frequency of 128 kHz for a signal frequency of 1 kHz. This system achieves a SNR of 67.3301 dB.



Output of integrator for sine wave



Output of self oscillating sigma delta modulator for ramp input



First order self oscillating sigma delta modulator