Design and Analysis of 10-bit Pipelined ADC using 1.5-bit MDAC

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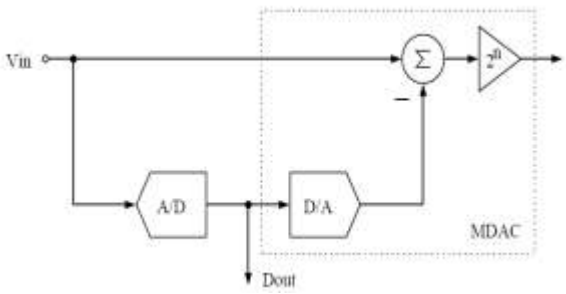
Abstract:

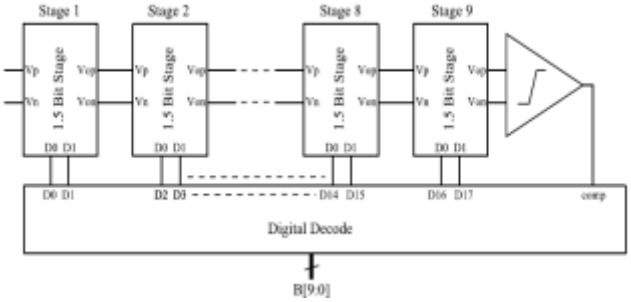
Analog to Digital Converter (ADC) design has been an active research topic over the past few decades, as the scaling down of Complementary Metal-Oxide-Semiconductor (CMOS) Integrated Circuit (IC) fabrication process offers continuing room for performance improvement. Various ADC architectures have been proposed by researchers, including Flash, Successive Approximation, Sigma-Delta and Pipeline. Among these architectures, Pipeline ADC offers moderate resolution at high conversion speed and is widely used in both civil and military applications. In this work, a 9 stage 10 bit, 1.8 V, 25 MSPs pipelined ADC architecture has been developed in 180 nm CMOS technology.

Pipelined ADC Literature has been reviewed and low power architecture has been identified for 10 bit Pipelined ADC based on 1.5 bit MDAC. All the sub blocks of pipelined ADC such as Sample and Hold circuit, 1.5 bit Flash ADC, Encoder, 1.5 bit DAC, Subtractor, Integrator and 1.5 bit MDAC have been identified, designed and analysed properly for correctness and performance efficiency. The top level 10-bit Pipelined ADC has been developed by integrating all the sub blocks with digital error correction circuit.

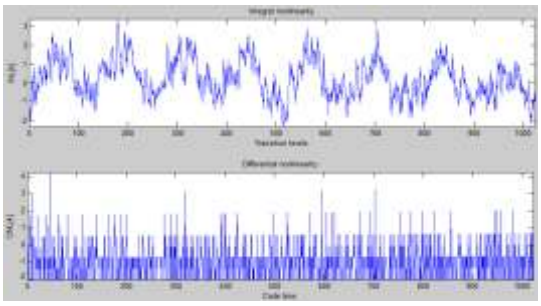
The simulation results of sub blocks show Opamp has 64 dB of gain and 65 degrees of Phase Margin. Correctness of MDAC part has been verified by comparing to transfer function of 1.5 bit per stage MDAC for DC and sine wave AC inputs. Top level design of Pipelined ADC has been simulated for 2 MHz input signal.



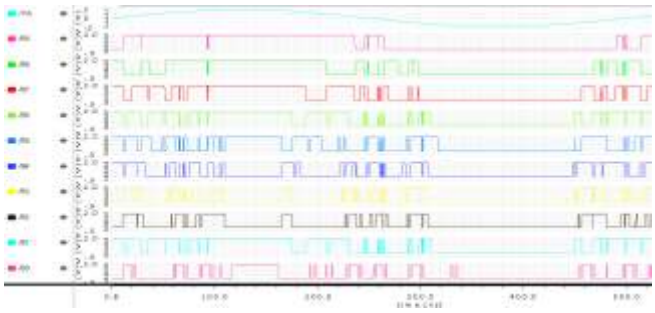
1.5-bit MDAC architecture



10-bit pipelined ADC architecture



INL DNL profile



Developed 10-bit ADC output simulation