Design and Implementation of Parallel NoC Architecture for AES Algorithm on FPGA

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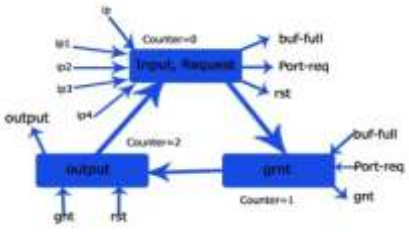
Abstract:

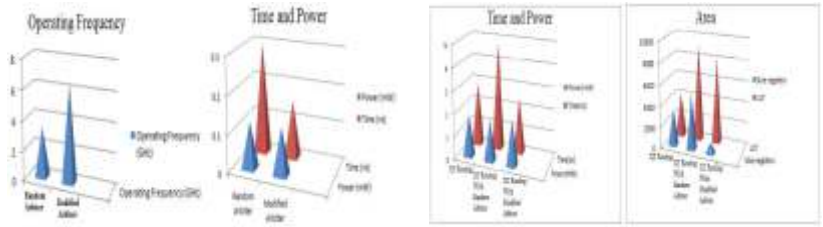
Network on chip (NoC) is the scalable platform where billion transistors have been integrated on to a single chip. NoC architecture is a m × n mesh architecture of processing elements where resources are placed on the slots formed by the switches. Each switch is connected to one resource and four neighboring switches, and each resource is connected to one switch. A resource can be a processor core, memory, or any other intellectual property (IP) block, which fits into the available slot and complies with the interface of the NoC. The NoC architecture is an on-chip communication infrastructure which comply OSI protocol stack.

Existing XY algorithm has a deadlock issue and head of line blocking problem which reduces the efficiency of system. In this work, a modified routing logic has been proposed and developed for NoC architecture to overcome drawbacks of XY algorithm. The modified arbiter has the 3 states of operation such as input, grant and output states. It solves dead lock problem by checking buffer status of input ports in each clock cycle and adjusts its input port dynamically based on which the request and grant signals has been generated. Head of line blocking problem has been solved by authorizing the input port for transferring data preferentially if the buffer port is full.

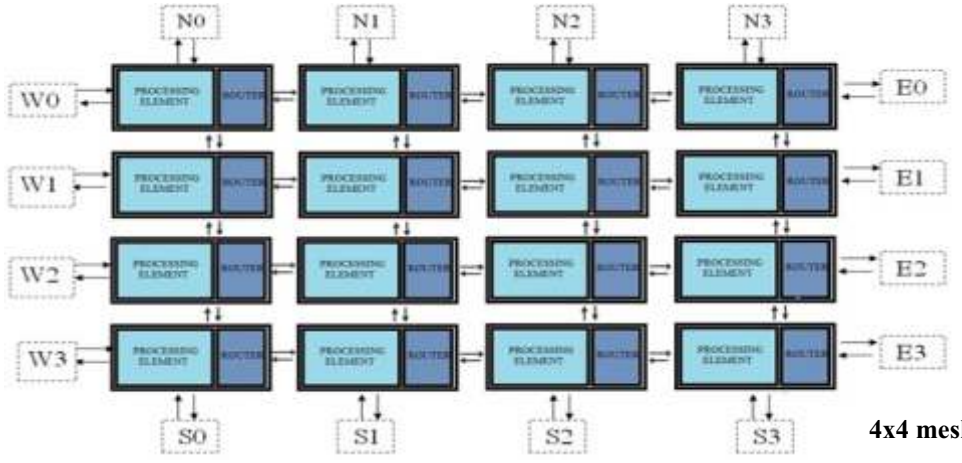
The developed NoC architecture is integrated with Advanced Encryption Standard (AES) algorithm. Maximum operating frequency of developed NoC architecture with modified arbiter routing logic is obtained as 404 MHz. The proposed arbiter routing logic requires 2.47 ns for output response which is faster than existing routing logic. It consumes 1.9 mW of power which is more than random arbiter logic (1.8 mW). With a tradeoff between speed and power, NoC architecture with high performance in terms of speed and hardware resource utilization has been developed using XY algorithm with proposed modified arbiter logic.



Functional block diagram



Performance comparison results



4x4 mesh architecture of noc