Design and Implementation of DDR SDRAM Memory Controller on FPGA

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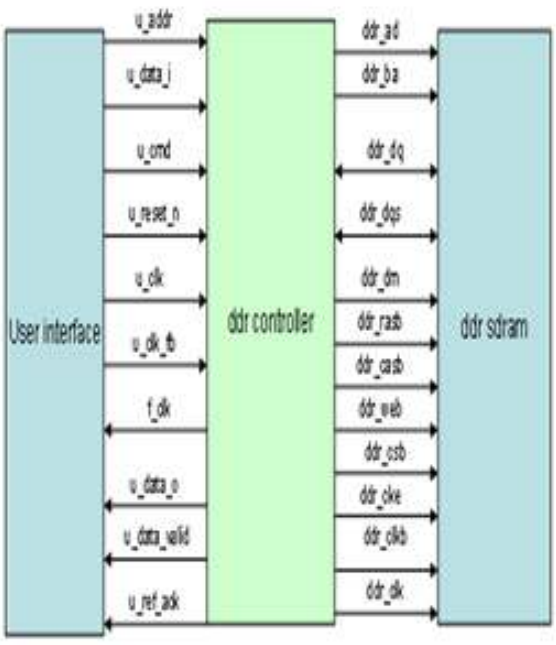
Abstract:

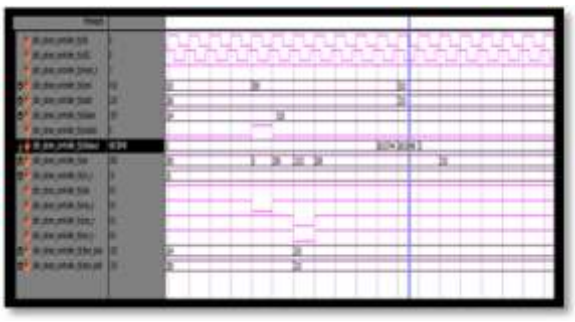
Synchronous Dynamic RAM (SDRAM) is preferred in embedded system memory design because of its speed and pipeline capability. In high end applications, like Microprocessors there will be specific built in peripherals to provide the interface to the SDRAM. But for other applications, the system designer must design a specific memory controller to provide command signals for memory refresh, read and write operation and initializing SDRAM. The controller is located between the SDRAM and the bus master, which minimizes the effort to deal with the SDRAM memory by providing a simple system to interact with the bus master.

This work focuses on designing the memory blocks and Double Data Rate (DDR) SDRAM memory controller. Finite State Machine (FSM) initializes the memory controller by passing on a sequence of command signals. The proposed SDRAM Memory Controller is used to enhance the computational performance on the FPGA, because FPGA has stand alone has its inbuilt memory with an aspect ratio of 4k x 4k which is limited for complex computations.

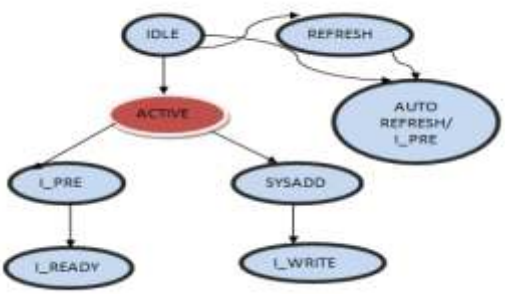
Implementation of DDR SDRAM memory controller on FPGA, the data handling capability and computational performance have improved by increasing the memory size to 1024 bytes at an operating frequency of 200 MHz. FPGA will play an important role in performing these complex computations effectively. The developed blocks are tested for matrix computation on FPGA.



Block diagram of DDR SDRAM



Simulation results of DDR SDRAM



FSM daigram