Design and Development of a Software Defined Radio (SDR) Receiver

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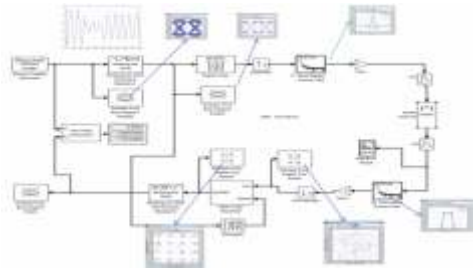
Abstract:

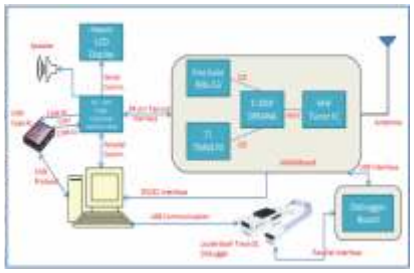
Traditional hardware based radio devices limit cross-functionality and can only be modified through physical intervention leading to higher production costs and minimal flexibility in supporting multiple waveform standards. In order to provide an efficient and comparatively inexpensive solution to this problem allowing multi-mode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades, a new technology was evolved called Software Defined Radio (SDR). While several proprietary and commercial implementations are available, there are very few implementations of functional SDR transceiver discussed in open literature.

This project deals with the modelling, software simulation and hardware realisation of an SDR receiver with configurable demodulation on a general purpose processor. Energy detection based spectrum sensing, channel equaliser, RRC filter; synchronisation and demodulation blocks are designed and developed as part of the SDR receiver. The developed receiver dynamically switches between demodulation techniques. The software simulation of the SDR system is carried out with MATLAB/Simulink and the hardware simulation is carried out using Xilinx Sys Gen blocks. The hardware implementation is realised by porting the required firmware and configuring the hardware using Freescale iMX53, TI TMS470 controller and CDSP DIRANA for VHF II (FM) frequency ranges.

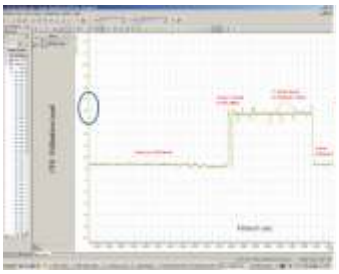
The performance and results under various conditions of input and test scenarios are seen and validated. Results with different channel characteristics, Quality of Signal, Turnaround Time, Stack usage and ER comparisons are also evaluated. It is observed that the SDR receiver using QAM demodulation technique yields around 15% better Signal Quality when compared to QPSK as characterised by the ER. However, it also has around 20% longer turnaround time and utilises around 10-15% higher CPU Load than the QPSK demodulation.

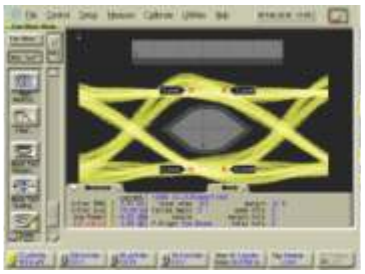


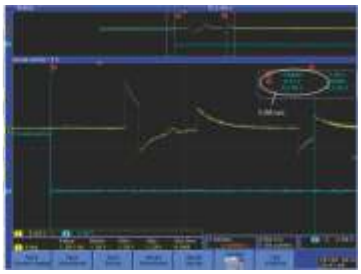
Software model of SDR transceiver



Hardware setup and block diagram of SDR receiver







CPU load measurements, captured eye diagram for received signal and timing diagram of SDR receiver