Design and Implementation of a SystemC Based Cycle Accurate RISC Simulator

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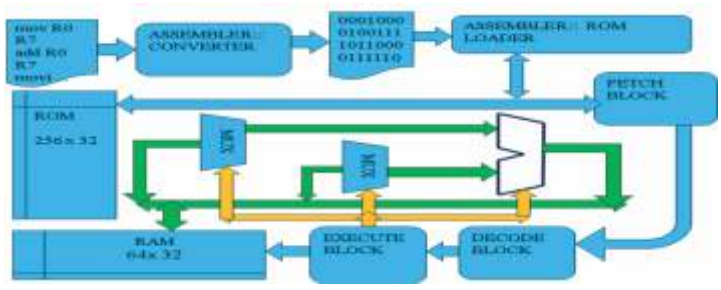
Abstract:

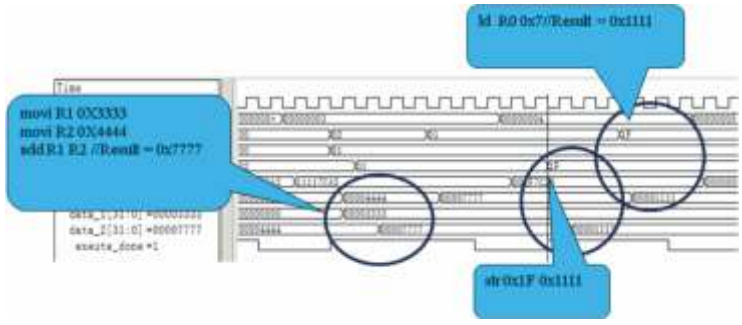
Architectural simulators are used to model computer components to predict their behaviour and performance, without building or using costly physical hardware systems. The traditional software design flow relies on hardware to be developed first which leads to delayed time to market and need for careful sequencing of hardware and software development activities. Virtual hardware simulator models elevate these problems. However, these simulators have to be cycle-accurate, accurately mimic their hardware counterparts in terms of not only their behaviour but also in their timing.

In this project, a scalable cycle-accurate RISC processor hardware simulator model is developed and its hardware architectural performance is analysed using behaviour simulations. The design flow of the model is split into software and hardware sections. The software section, which includes the assembler and the ROM loader, is designed to convert assembly language into machine level language. The hardware section includes processor core such as ROM, RAM, ALU, FETCH, DECODE, and EXECUTE blocks. The model has been designed using SC_THREADS in SystemC which enables actual behaviour of real time hardware. The graphical transaction tracing has been performed through GTKWave.

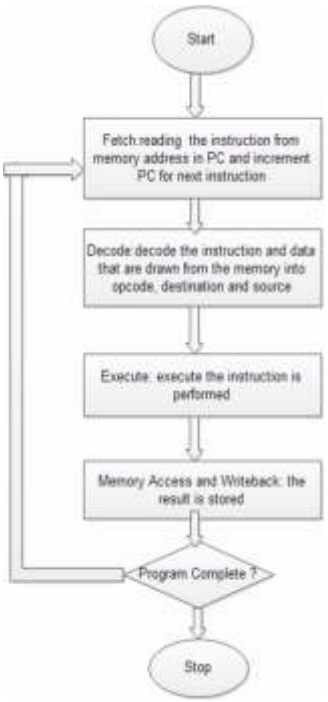
The developed model simulates modern RISC processor behavior with on-chip memories having the write cycle time of 1 processor clocks and the read cycle time of 2 processor clocks. It is measured to produce a latency of 40 ns and a throughput of 1 instruction/cycle at a maximum speed of 25 MHz.



Cycle accurate RISC simulator architecture



Execute to RAM WB



Data flow