Design and Development of Reconfigurable Colour Correction Slave Peripheral and Co-Processor Modules

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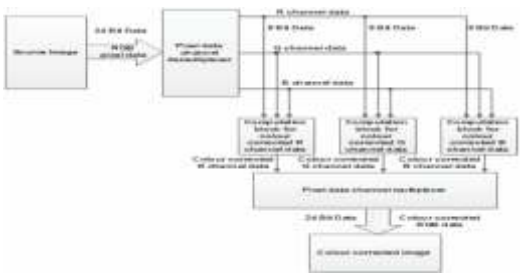
Abstract:

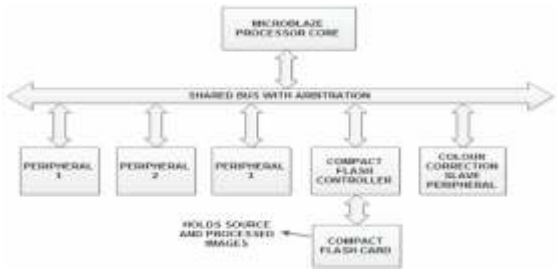
The colour intensity and natural contents of the digital images occasionally need boosting as per the capture scene due to luminance issues, pixel crosstalk, colour channel overlap issues and the inconsistent results due to error prone CMOS sensors of the optical image capture device. The Colour Correction logic can handle the requirements to process the faulty images and bring out realistic results as perceived by the human vision. The detailed understanding of the various computational algorithms is essential for venturing into design and implementation of the application.

In this project, four unique algorithms for Colour Correction are considered. The algorithm that has least computational requirements and run-time is chosen. The specifications for the design are built based on the system components, technology and infrastructure available for prototyping. The modelling of application starts with RTL design of the Colour Correction model using the bayer mask values to process individual R, G and B channels. The algorithm is modelled and run as a software application in a MicroBlaze processor system. The processing logic of the application is modelled as a slave peripheral and co-processor modules using the standalone IP core and integrated into MicroBlaze system. The corresponding variants of MicroBlaze systems are driven from application layer with source image data. The performance analysis is conducted by comparing throughput results of slave peripheral and co-processor modules.

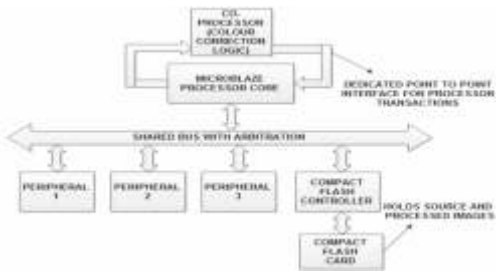
Ideal Colour Corrected images are obtained through functional simulation of standalone IP and resource utilization reports consists of 18 CLB's. The resource utilization of slave peripheral and co-processor module based systems vary by 2 percent. The performance analysis results give clear indications of the throughput improvement achieved using the co-processor implementation due to optimisation of latencies and arbitration delays, making it ideal for imaging and media applications. The performance can be further improved by processing multiple pixels parallely and providing DMA support for co-processor for seamless access to memory holding source images, and out-of order execution into the developed architecture and analyse its effect on time predictability.



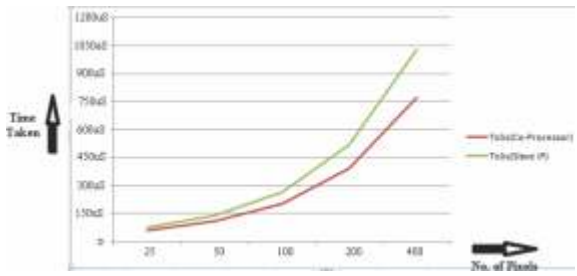
RTL Diagram for standalone IP logic



Colour correction logic as a slave peripheral



Colour correction logic as a co-processor



Performance analysis graph