Design and Simulation of Victim Cache and Skewed Associative Cache for RISC Architecture

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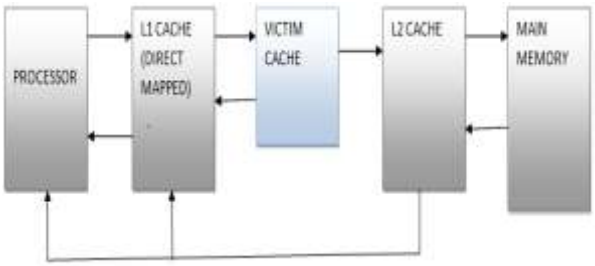
Abstract:

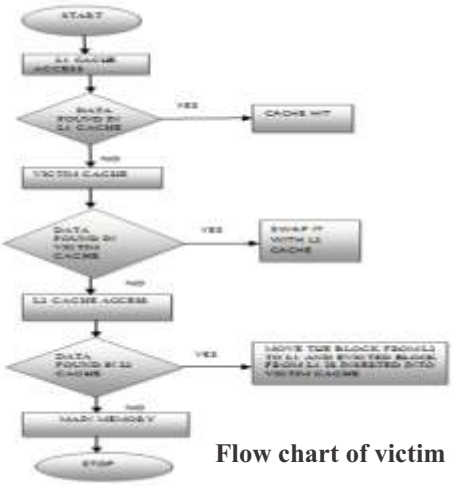
Speed is the major limiting factor for the performance of the computer with which the data can be moved between processor and memory. So cache memory was placed between the main memory and processor. Several mapping techniques were used to map data into cache memory. Since L1 cache is direct mapped it has one-to-one relation, different address of data will conflict for same location in L1 cache and hence there is a miss called conflict misses which leads to miss penalty thus decreasing the performance.

In this project, a new two cache schemes were used like victim cache and skewed associative cache to basic RISC architecture to hold the conflict misses. Victim cache is fully associative cache and its size is small compared to L1 cache, it is placed next to L1 instruction cache to hold the evicted block because of conflict miss or replaced block from L1 cache. Another new cache scheme is skewed associative cache, where two mapping function is used to map the address into different banks with different location which is unlike in conventional cache scheme.

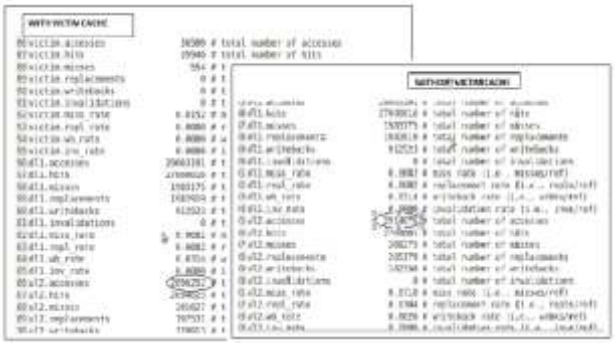
The developed cache schemes was simulated and analyzed using the sim-cache functional simulator of simplescalar tool. The obtained results are analyzed for performance. Victim cache is able to solve nearly 90% of conflict misses and reduce access rate of L2 cache. But with skewed associative cache, tool made us to implement only single mapping function in which not able to achieve the required result.



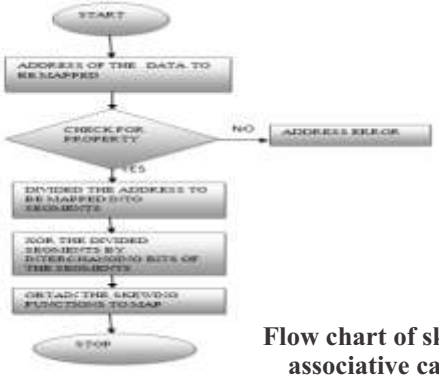
Block diagram of victim cache



Flow chart of victim cache



Cache statistics with and without victim cache



Flow chart of skewed associative cache