Design, Implementation and Analysis of Efficient Viterbi Decoder Architecture

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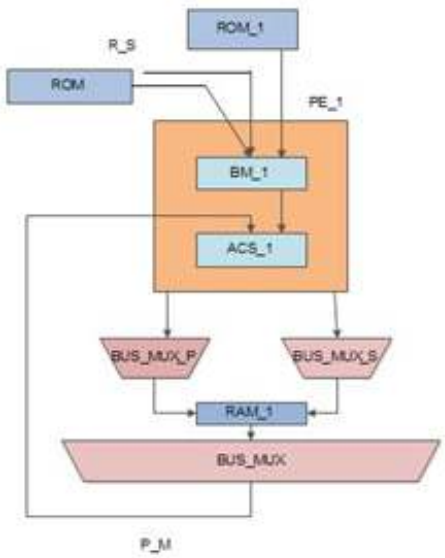
Abstract:

Recent world embedded communication system got many applications. In these communication system, message transferred at the transmitter is expected same as at receiver, but there are losses in the channel hence channel coding plays a vital role in digital communication systems. Most of the communication systems use Convolutional encoder for compensating the error induced by the Additive White Guassian noise, channel fading and quantization. The Viterbi algorithm is a well known efficient method for the Maximum Likelihood decoding for convolutional encoder. The combination of the Convolutional encoder and Viterbi decoder provides forward error correction scheme.

In this project, efficient Viterbi decoder of constraint length 9 and ½ coder rate architecture is design and implemented and analysed. Viterbi algorithm is the better maximum likelihood decoder and the loss of information and information containing error at receiver motivated to develop the efficient Viterbi decoding architecture so that the better bit error rate can be achieved. The Viterbi algorithm is organized in the form of matrix vector computation and is implemented in hardware based on systolic architecture. This implementation includes the strongly connected trellis method is used to improve the efficiency of hardware utilization and speed of the decoding. Novel systolic array architecture with arithmetic pipelining, time multiplexing is developed and clock-data skews are avoided. The proposed design is implemented using FPGA, results in power dissipation by lowering the switching activities in ACS unit. The VHDL code for efficient Viterbi decoder has been implemented and analysed the design using systolic architecture. The developed VHDL code is verified by writing test benches and test-circuit to cover all the possible corner cases in ISE simulation tool.

The design of an efficient Viterbi decoder results in lesser hardware resources utilization and the execution of VHDL code of design processing frequency are of 190.491 MHz and 175 mW of power is consumed. The proposed an efficient Viterbi decoder using novel architecture is 56% and 55% better when compared to the traditional Viterbi decoder using butterfly architectures in terms of power and speed respectively.



Systolic architectural design of single processing element of Viterbi decoder

Results of convolutional encoder and Viterbi decoder