Design and Simulation Analysis of an Efficient Software Prefetching Method for Cache Memory

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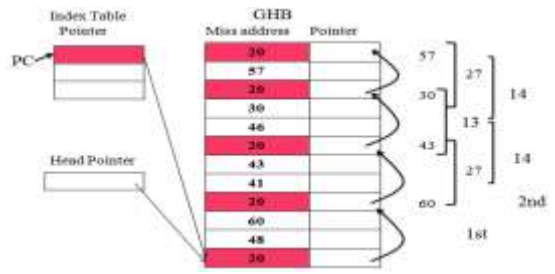
Abstract:

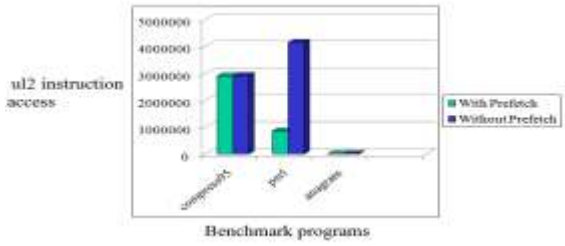
For read and write operations, there is a large performance gap between the processor and the main memory. Caching is the principle technique used to overcome this gap and improve the system performance. However, cache misses continue to degrade the performance benefit achieved through caching. Prefetching memory blocks into CPU caches has long been known as an effective solution for reducing such degradation. In this thesis, an efficient software prefetching method for cache memory is developed for PISA architecture in Simple Scalar architecture simulation tool.

In this project, a survey is conducted to identify existing prefetching mechanisms. A new structure for implementing cache prefetching is proposed based on the survey conducted. This structure is implemented in Simple Scalar tool and its performance is analyzed by simulation. The structure is based on a Global History Buffer that holds the most recent miss addresses in FIFO order. The existing Aggressive prefetching algorithm is designed using Global history which gives the better prefetching enhancement of SPEC benchmark programs. The miss ratio in level 2 cache are considerably reduced after adding prefetch cache between the level 1 and level 2 caches. The developed prefetching algorithm is simulated and analyzed using SimpleScalar simulator.

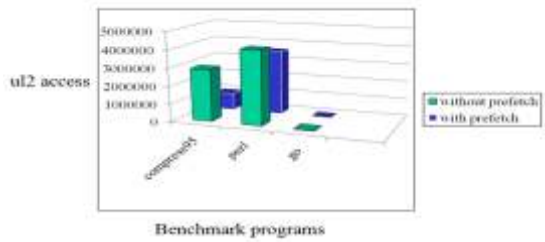
Simulated results obtained from SPEC95 benchmarks shows that the developed prefetching method predicts the prefetching address and thereby reducing the number of access to the level 2 caches. The performance enhancement is greater for perl.ss and go.ss benchmark programs for il1 cache when compared to dl1 cache. The average performance enhancement for il1 cache is 2.62 times better than without prefetching and for dl1 cache is 1.60 times better than without prefetching. The developed method is suitable for both data and instruction caches. The aggressive prefetching with GHB performs well than the other prefetching algorithms. The future work will be based on adapting different prefetching algorithms using GHB and to define efficiency criteria for prefetching algorithms.



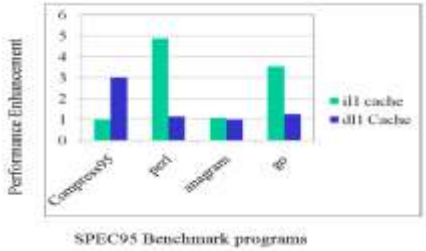
Global history buffer



Ul2 access of each benchmark programs for il1 cache



Ul2 access of each benchmark programs for dl1



Performance enhancement of il1 and dl1 cache after prefetch