Design and Development of Systolic and CORDIC Architectures for MIMO STBC

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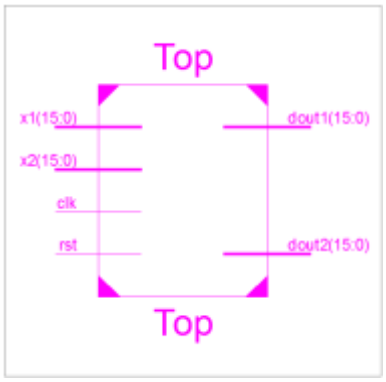
Abstract:

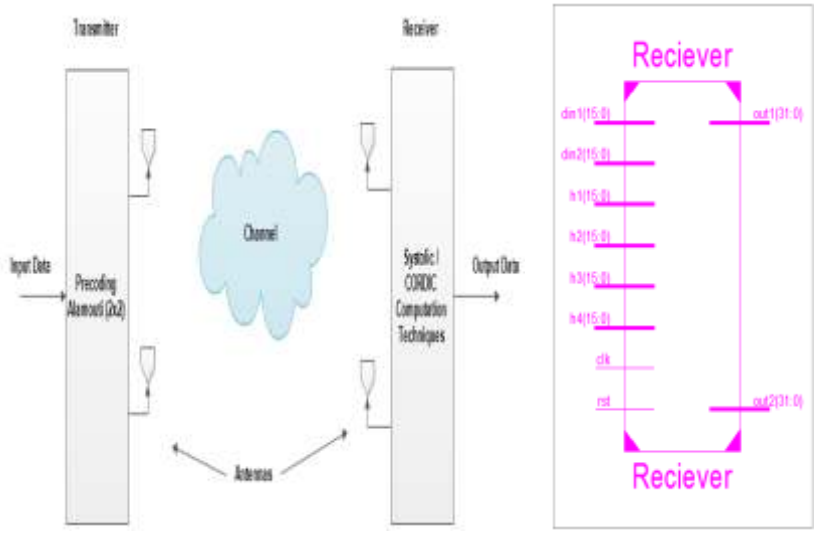
This project focuses on designing and implementing FPGA-based Multiple Input Multiple Output (MIMO) system using Space Time Block Coding (STBC) algorithm based on the Systolic and CORDIC architectures to solve some typical operations as well as transcendental equations such as addition and multiplication. Normally, the Space Time Block Coding (STBC) i.e. Alamouti algorithm helps to increase the capacity without increasing the total transmission power.

In this project, multi-antenna transmission schemes, using multiple antennas at the transmitter and receiver, have been proposed as a way to fulfill the demand for developing receiver architectures. The aim of this project is to implement a particular multi-antenna scheme, a 2×2 Alamouti code. A MIMO encoder and decoder is designed by Systolic and CORIDC architectures. The designs have been verified by simulation of VHDL code. The simulation results have been favorable with the MIMO scheme. The Systolic computes these equations parallelly with pipelined architecture. This architecture utilizes fewer resources compared to other conventional, but as computation complexity increases the architectural design issues will also increase. The CORDIC architecture is developed for computation of MIMO STBC equation. The conversion of complex number into its conjugate is carried out by CORDIC method and remaining computations are performed with Systolic method.

The performance analysis is carried out with respect to resource utilisation; power and speed are same for both the architectures as 1.043 mW and 660.323 MHz respectively. The CORDIC architecture uses lesser resources and hence a better architecture.



Top level RTL schematic for STBC encoder



Block diagram of Alamouti 2x2 transceiver system & RTL for systolic architecture